L6759D

3+1 dual controller for VR12 with PMBus

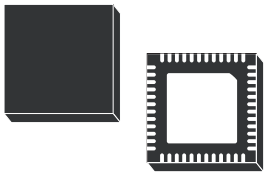
Datasheet — production data

Features

- VR12 compliant with 25 MHz SVID bus Rev1.5
  - SerialVID with programmable IMAX, TMAX, VBOOT, ADDRESS
- Second generation LTB Technology™
- Flexible driver/DrMOS support
- JMode support
- Fully configurable through PMBus
- Dual controller:
  - 3-phase for VDDQ
  - 1-phase for VTT
- Single NTC design for TM, LL and Imon thermal compensation
- VFDE and GDC - gate drive control for efficiency optimization
- DPM - dynamic phase management
- Dual remote sense
- 0.5% output voltage accuracy
- Full-differential current sense across DCR
- AVP - adaptive voltage positioning
- Dual independent adjustable oscillator
- Dual current monitor
- Pre-biased output management
- Average and per-phase OC protection
- OV, UV and FB disconnection protection
- Dual VR_RDY
- VFQFPN48 6x6 mm package

Application

- DDR3 memory supply for VR12 servers



VFQFPN48 - 6x6mm

Description

The L6759D is a dual controller designed to power Intel's VR12 processor memories: all required parameters are programmable through dedicated pin-strapping and PMBus interface.

The device features 3-phase programmable operation for the multi-phase section and a single-phase with independent control loops. Single-phase (VTT) reference is always tracking multi-phases (VDDQ) scaled by a factor of 2.

The L6759D supports power state transitions featuring VFDE, programmable DPM and GDC maintaining the best efficiency over all loading conditions without compromising transient response.

The device assures fast and independent protection against load overcurrent, under/overvoltage and feedback disconnections.

The device is available in a VFQFPN48 6x6 mm package.

Table 1. Device summary

Order code	Package	Packing
L6759D	VFQFPN48 6x6mm	Tray
L6759DTR		Tape and reel

This is information on a product in full production. www.st.com

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1 Typical application circuit and block diagram

1.1 Application circuit

Figure 1. Typical 3-phase application circuit

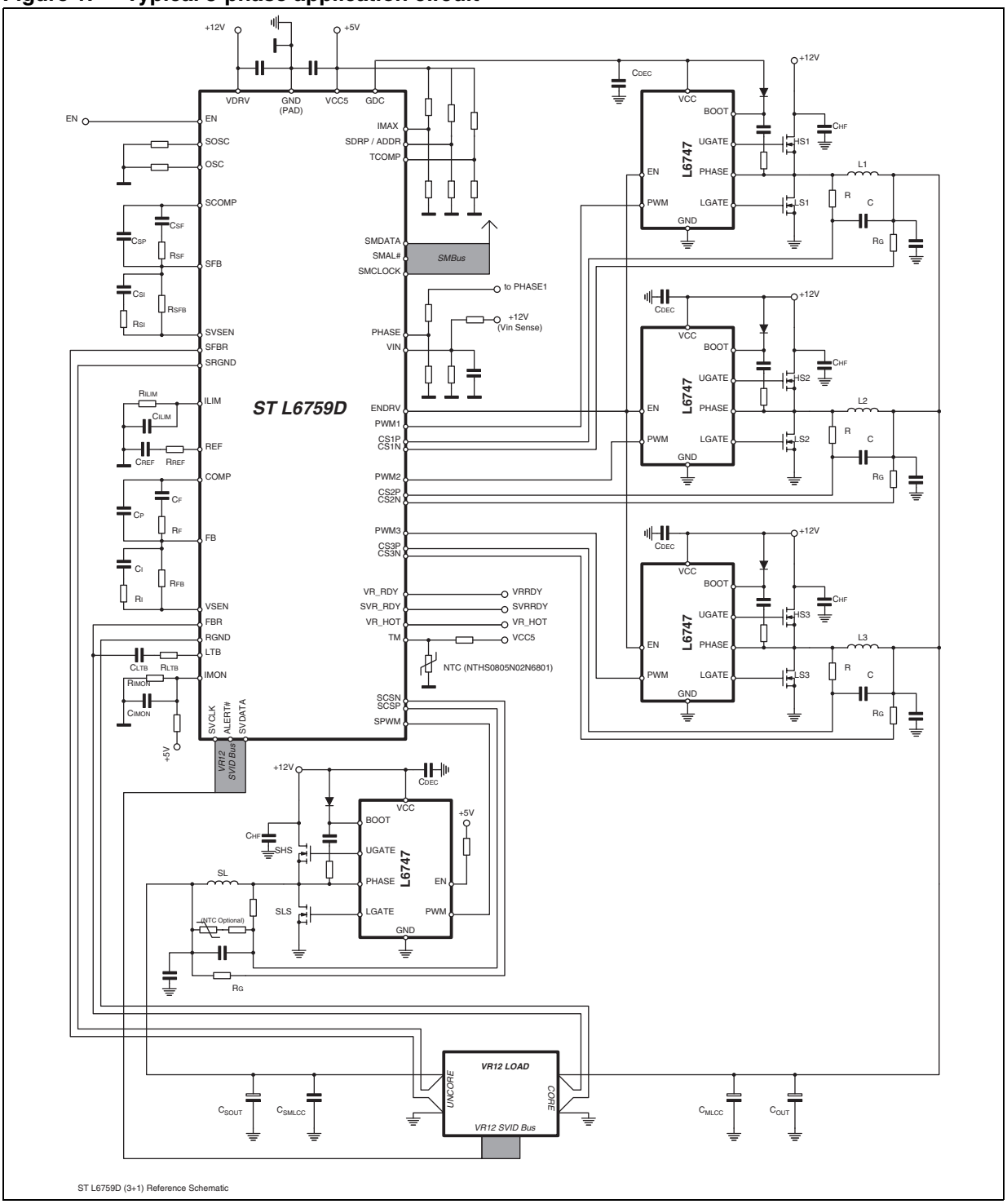
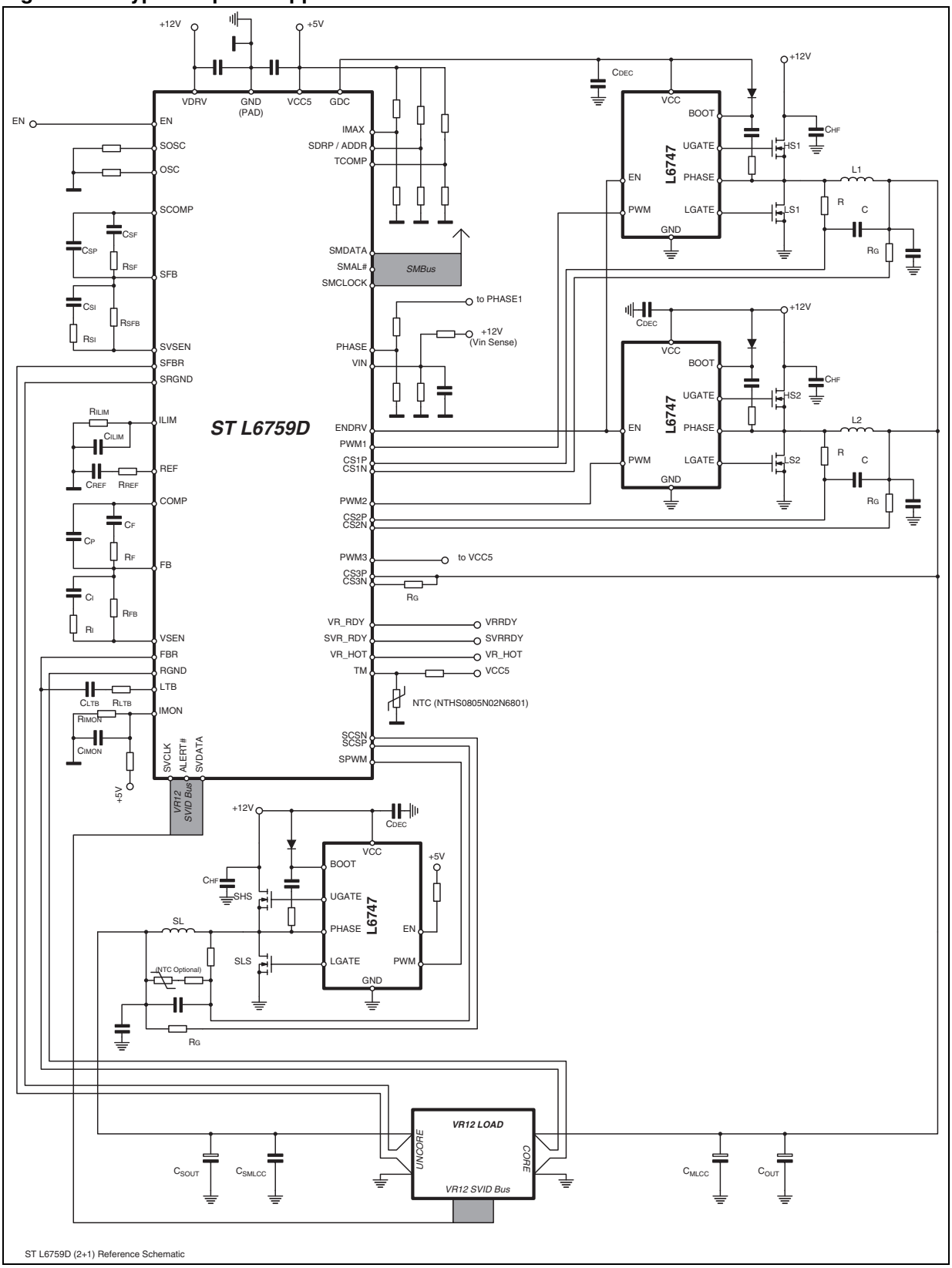


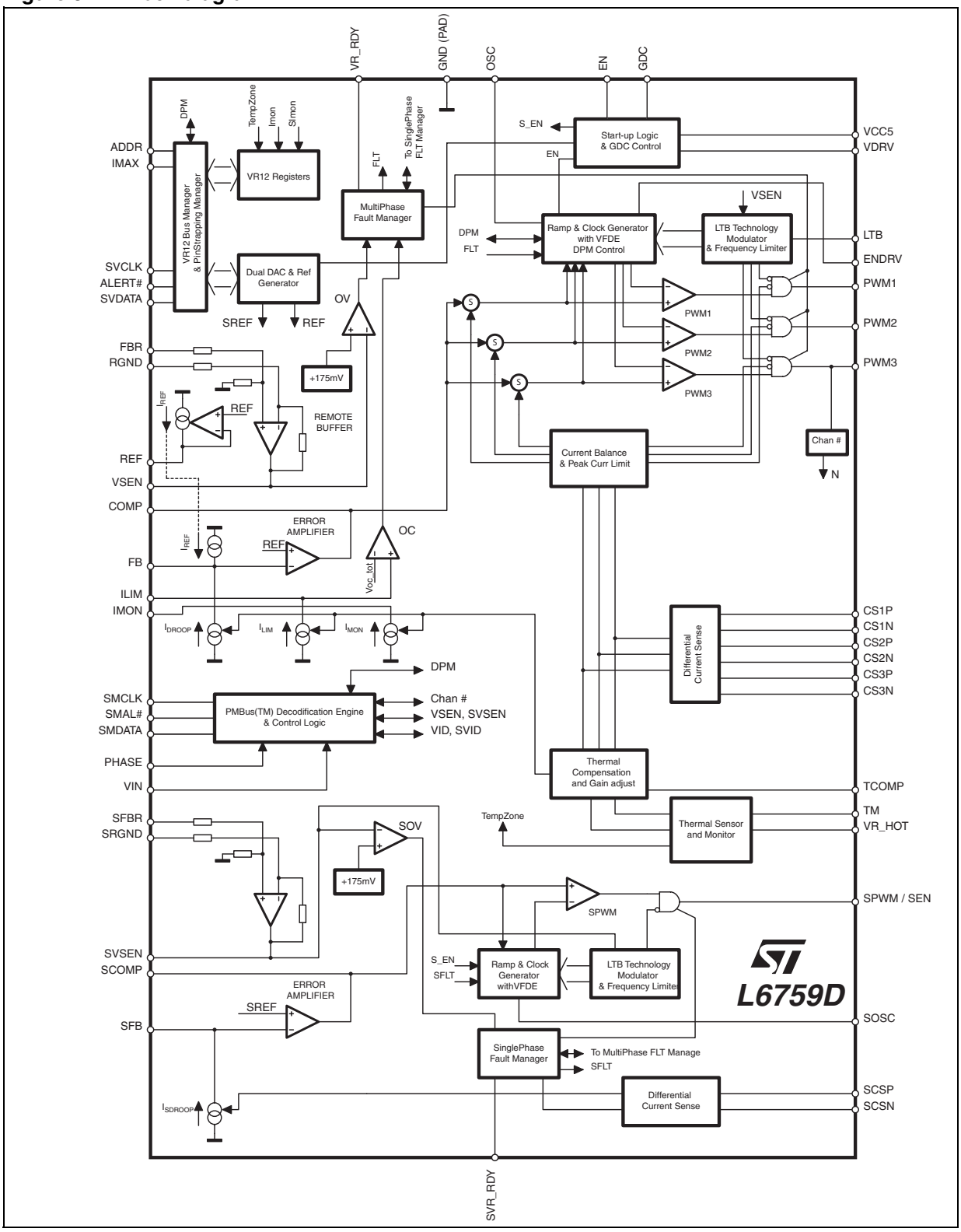
Figure 2. Typical 2-phase application circuit



ST L6759D (2+1) Reference Schematic

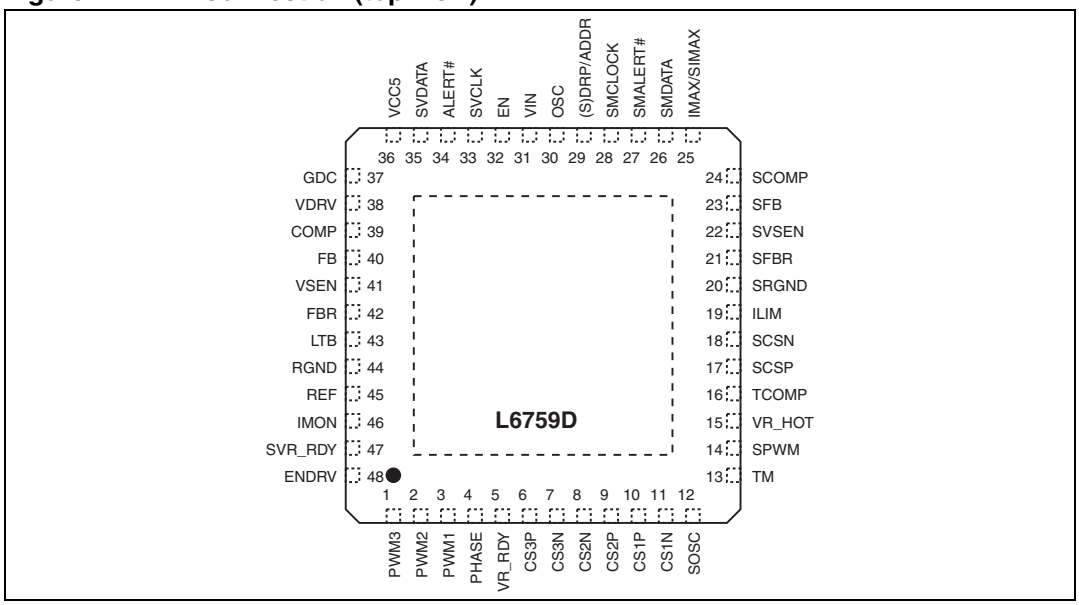
1.2 Block diagram

Figure 3. Block diagram



2 Pin description and connection diagrams

Figure 4. Pin connection (top view)



2.1 Pin description

Table 2. Pin description

Pin#	Name		Function
1 to 3	PWM3 to PWM1	Multi-phase section	PWM outputs. Connect to multi-phase external drivers PWM input. These pins are also used to configure HiZ levels for compatibility with drivers and DrMOS. During normal operations the device is able to manage the HiZ status by setting and holding the PWMx pin to a pre-defined fixed voltage. Connect PWM3 to 5 V through 1 kW resistor to program 2-phase operation.
4	PHASE		Connect through resistor divider to Channel1 multi-phase switching node.
5	VR_RDY		VR ready. Open drain output set free after SS has finished in multi-phase and pulled low when triggering any protection on the multi-phase section. Pull up to a voltage lower than 3.3 V (typ.), if not used it can be left floating.
6	CS3P		Channel 3 current sense positive input. Connect through an R-C filter to the phase-side of the channel 3 inductor. When working at 2-phase, short to the regulated voltage.
7	CS3N		Channel 3 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. When working at 2-phase, still connect through Rg to CS3P and then to the regulated voltage. Filter the output-side of Rg with 100 nF (typ.) to GND.

Table 2. Pin description (continued)

Pin#	Name		Function
8	CS2N	Multi-phase section	Channel 2 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND.
9	CS2P		Channel 2 current sense positive input. Connect through an R-C filter to the phase-side of the channel 2 inductor.
10	CS1P		Channel 1 current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor.
11	CS1N		Channel 1 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND.
12	SOSC	Single-phase section	Oscillator pin. It allows the programming of the switching frequency F_{SSW} for the single-phase section. The pin is internally set to 1.02 V, frequency for single-phase is programmed according to the resistor connected to GND or VCC with a gain of 11.5 kHz/µA. Leaving the pin floating programs a switching frequency of 230 kHz. See *Section 10* for details.
13	TM	Multi-phase section	Thermal monitor sensor. Connect with the proper network embedding NTC to the multi-phase power section. The IC senses the power section temperature and uses the information to define the VR_HOT signal and temperature zone register. By programming proper TCOMP gain, the IC also implements load-line thermal compensation for the multi-phase section. In JMode, the pin disables the single-phase section if shorted to GND. Pull up to VCC5 with 1 kΩ to disable the thermal sensor. See *Section 6* for details.
14	SPWM / SEN	Single-phase section	PWM output. Connect to single-phase external driver PWM input. During normal operations the device is able to manage HiZ status by setting and holding the SPWM pin to a fixed voltage defined by PWMx strapping. Connect to VCC5 with 1 kΩ to disable the single-phase section.
15	VR_HOT		Voltage regulator HOT. Open drain output, this is an alarm signal asserted by the controller when the temperature sensed through the TM pin exceeds TMAX (active low). See *Section 6* for details.
16	TCOMP	Multi-phase section	Thermal monitor sensor gain. Connect the proper resistor divider between VCC5 and GND to define the gain to apply to the signal sensed by TM to implement thermal compensation for the multi-phase section. Short to GND to disable temperature compensation (but not thermal monitor). See *Section 6* for details.
17	SCSP	Single-phase section	Single-phase section current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor.
18	SCSN		Single-phase section current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND.

Table 2. Pin description (continued)

Pin#	Name		Function
19	I_{LIM}	Single-phase section	Multi-phase section current limit. A current proportional to the multi-phase load current is sourced from this pin. Connect through a resistor R_{LIM} to GND. When the pin voltage reaches 2.5 V, the overcurrent protection is set and the IC latches. Filter through C_{LIM} to GND to delay OC intervention.
20	SRGND		Remote buffer ground sense. Connect to the negative side of the single-phase load to perform remote sense.
21	SFBR		Remote buffer positive sense. Connect to the positive side of the single-phase load to perform remote sense.
22	SVSEN		Remote buffer output. Output voltage monitor, manages OV and UV protection. Connect with a resistor R_{SFB} // (R_{SI} - C_{SI}) to SFB.
23	SFB		Error amplifier inverting input. Connect with a resistor R_{SFB} // (R_{SI} - C_{SI}) to SVSEN and with an (R_{SF} - C_{SF})// C_{SH} to SCOMP.
24	SCOMP		Error amplifier output. Connect with an (R_{SF} - C_{SF})// C_{SH} to SFB. The device cannot be disabled by pulling low this pin.
25	IMAX	Pin-strapping	Connect a resistor divider to GND/VCC5 in order to define the IMAX register. JMode and BOOT voltage can be controlled through this pin. See *Table 6* and *Section 6* for details.
26	SMDATA	PMBus	PMBus data.
27	SMAL#		PMBus alert.
28	SMCLOCK		PMBus clock.
29	ADDR	Pin-strapping	Connect a resistor divider to GND/VCC5 in order to define the IC address, to define the GDC and DPM thresholds and to control the droop function on multi-phase. See *Table 6* and *Section 6* for details.
30	OSC	Multi-phase section	Oscillator pin. It allows the programming of the switching frequency F_{SW} for the multi-phase section. The pin is internally set to 1.02 V, the frequency for multi-phase is programmed according to the resistor connected to GND or VCC with a gain of 10 kHz/µA. Leaving the pin floating programs a switching frequency of 200 kHz per phase. The effective frequency observable on the load results being multiplied by the number of active phases N. See *Section 10* for details.
31	VIN		Input voltage monitor. Connect to input voltage monitor point through a divider R_{UP} / R_{DOWN} to perform VIN sense through PMBus (R_{UP} = 118.5 kΩ; R_{DOWN} = 10 kΩ typ.). See *Section 12.3* for details.

Table 2. Pin description (continued)

Pin#	Name		Function
32	EN		VTT level sensitive enable pin (3.3 V compatible). Pull low to disable the device, pull up above the turn-on threshold to enable the controller.
33	SVCLK	SVI BUS	Serial clock.
34	ALERT#		Alert.
35	SVDATA		Serial data.
36	VCC5		Main IC power supply. Operative voltage is 5 V ±5%. Filter with 1 µF MLCC to GND (typ.).
37	GDC		Gate drive control pin. Used for efficiency optimization, see *Section 9* for details. If not used, it can be left floating. Always filter with 1 µF MLCC to GND.
38	VDRV		Driving voltage for external drivers. Connect to the selected voltage rail to drive the external MOSFET when in maximum power conditions. IC switches GDC voltage between VDRV and VCC5 to implement efficiency optimization according to selected strategies.
39	COMP / ADDR	Multi-phase section	Error amplifier output. Connect with an (R_F - C_F)// C_P to FB. The device cannot be disabled by pulling low this pin. Connect R_{COMP} to GND to extend PMBus addressing range (see *Table 6*).
40	FB		Error amplifier inverting input. Connect with a resistor R_{FB} // (R_I - C_I) to VSEN and with an (R_F - C_F)// C_P to COMP.
41	VSEN		Output voltage monitor, manages OV and UV protection. Connect to the positive side of the load to perform remote sense.
42	FBR		Remote buffer positive sense. Connect to the positive side of the multi-phase load to perform remote sense.
43	LTB		Load transient boost technology® input pin. See *Section 11.2* for details.
44	RGND		Remote ground sense. Connect to the negative side of the multi-phase load to perform remote sense.
45	REF		The reference used for the multi-phase section regulation is available on this pin with -125 mV offset. Connect through an R_{REF}-C_{REF} to GND to optimize DVID transitions. Connect through R_{OS} resistor to FB pin to implement small positive offset to the regulation.
46	IMON		Current monitor output. A current proportional to the multi-phase load current is sourced from this pin. Connect through a resistor R_{MON} to GND. The information available on this pin is used for the current reporting and DPM. The pin can be filtered through C_{IMON} to GND.

Table 2. Pin description (continued)

Pin#	Name		Function
47	SVR_RDY	Single-phase section	VR ready. Open drain output set free after SS has finished in single-phase section and pulled low when triggering any protection for the single-phase section.Pull up to a voltage lower than 3.3 V (typ.), if not used it can be left floating.
48	ENDRV	Multi-phase section	Enable driver. CMOS output driven high when the IC commands the drivers. Used in conjunction with the HiZ window on the PWMx pins to optimize the multi-phase section overall efficiency. Connect directly to external driver enable pin.
PAD	GND		GND connection. All internal references and logic are referenced to this pin. Filter to VCC with proper MLCC capacitor and connect to the PCB GND plane.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient (device soldered on 2s2p PC board)	40	°C/W
R_{thJC}	Thermal resistance junction to case	1	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	0 to 125	°C

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VDRV, GDC	to GND	-0.3 to 14	V
VCC5, TM, STM, SPWM, PWMx, SENDRV, ENDRV, SCOMP, COMP, SMDATA, SMAL#, SMCLK	to GND	-0.3 to 7	V
All other pins	to GND	-0.3 to 3.6	V

3.2 Electrical characteristics

V_{CC5} = 5 V ± 5%, T_J = 0 °C to 70 °C unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{VCC5}	VCC5 supply current	EN = high		28		mA
		EN = low		22		mA
$UVLO_{VCC5}$	VCC5 turn-ON	VCC5 rising			4.1	V
	VCC5 turn-OFF	VCC5 falling	3			V
$UVLO_{VDRV}$	VDRV turn-ON	VDRV rising			6	V
	VDRV turn-OFF	VDRV falling	3		4.1	V
$UVLO_{VIN}$	VIN turn-ON	VIN rising, R_{UP} = 118.5 kΩ; R_{DOWN} = 10 kΩ			6	V
	VIN turn-OFF	VIN falling, R_{UP} = 118.5 kΩ; R_{DOWN} = 10 kΩ	3		4.1	V
Oscillator, Soft-start and enable						
F_{SW}	Main oscillator accuracy	OSC = open	170	200	230	kHz
	Oscillator adjustability	R_{OSC} = 47 kΩ to GND	378	420	462	kHz
F_{SSW}	Main oscillator accuracy	SOSC = open	195	230	265	kHz
	Oscillator adjustability	R_{SOSC} = 47 kΩ to GND	432	480	528	kHz
ΔV_{OSC}	PWM ramp amplitude(1)			1.5		V
FAULT	Voltage at pin OSC, SSOSC	Latch active for related section	3			V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SOFT-START	SS time	Vboot > 0, from pin-strapping; multi-phase section	2.5			mV/µS
		Vboot > 0, from pin-strapping; single-phase section	1.25			mV/µS
		Vboot > 0, from pin-strapping; single-phase section, JMode ON	2.5			mV/µS
EN	Turn-ON	V_{EN} rising			0.6	V
	Turn-OFF	V_{EN} falling	0.4			V
	Leakage current			1		µA
SVI serial bus						
SVCLCK, SVDATA	Input high		0.65			V
	Input low				0.45	V
SVDATA, ALERT#	Voltage low (ACK)	I_{SINK} = -5 mA			50	mV
PMBus						
SMDATA, SMCLK	Input high		1.75			V
	Input low				1.45	V
SMAL#	Voltage low	I_{SINK} = -4 mA			13	Ω
Reference and DAC						
K_{VID}	V_{OUT} accuracy (MPhase)	FBR to V_{CORE}; RGND to GND_{CORE} VID>1.000 V	-0.5		0.5	%
K_{SVID}	V_{OUT} accuracy (SPhase)	JMODE=OFF; V_{UNCORE}/V_{CORE} SFBR to V_{UNCORE}; SRGND to GND_{UNCORE}; VID>1.000 V	0.49		0.51	
		JMODE=ON; SFBR to V_{UNCORE}; SRGND to GND_{UNCORE};	-5		5	mV
Δ_{DROOP}	LL accuracy (MPhase) 0 to full load	I_{INFOx} = 0 µA; N=3; R_G=866 Ω	-2.25		1.75	µA
		I_{INFOx} = 20 µA; N=3; R_G=866 Ω	-2.5		2.5	µA
k_{IMON}	IMON accuracy (MPhase)	I_{INFOx} = 0; N=3; R_G=866 Ω	0		0.75	µA
		I_{INFOx} = 20 µA; N=3; R_G=866 Ω	-1		1	µA
A_0	EA DC gain(1)			100		dB
SR	Slew-rate(1)	COMP to SGND = 10 pF		20		V/µs
DVID	Slew-rate fast	Multi-phase section	10			mV/µs
	Slew-rate slow		2.5			mV/µs
DVID	Slew-rate fast	Single-phase section	5			mV/µs
	Slew-rate slow		1.25			mV/µs

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
IMON ADC	GetReg(15h)	V(IMON) = 0.992 V		CC		Hex
	Accuracy		C0		CF	Hex
PWM outputs and ENDRV						
PWMx, SPWM	Output high	I = 1 mA		5		V
	Output low	I = -1 mA			0.2	V
I_{PWM1}	Test current	Sourced from pin, EN=0		10		µA
I_{PWM2}		Sourced from pin, EN=0		0		µA
$I_{PWM3, SPWM}$		Sourced from pin, EN=0		-10		µA
ENDRV	Voltage low	I_{ENDRV} = -4 mA			0.4	V
Protection (both sections)						
OVP	Overvoltage protection	VSEN rising; wrt Ref.	100		200	mV
UVP	Undervoltage protection	VSEN falling; wrt Ref; Ref > 500 mV	-525		-375	mV
FBR DISC	FB disconnection	V_{CS-} rising, above VSEN/SVSEN	650	700	750	mV
FBG DISC	FBG disconnection	FBR rising wrt VID	950	1000	1050	mV
VR_RDY, SVR_RDY	Voltage low	I_{SINK} = -4 mA			0.4	V
V_{OC_TOT}	OC threshold	V_{ILIM} rising, to GND	2.45	2.5	2.55	V
I_{OC_TH}	Constant current(1)	MPhase only		35		µA
VR_HOT	Voltage low	I_{SINK} = -4 mA			13	Ω
Gate drive control						
GDC	Max. current(1)	Any PS		200		mA
	Impedance	PS00h (GDC = VDRV)		6		Ω
		> PS00h (GDC = VCC5)		6		Ω

1. Guaranteed by design, not subject to test.

4 Device configuration and pin-strapping tables

The L6759D is fully compliant with Intel® VR12/IMVP7 SVID protocol Rev1.5, document # 456098. To guarantee proper device and CPU operations, refer to this document for bus design and layout guidelines. Different platforms may require different pull-up impedance on the SVI bus. Impedance matching and spacing between SVDATA, SVCLK, and ALERT# must be followed.

4.1 JMode

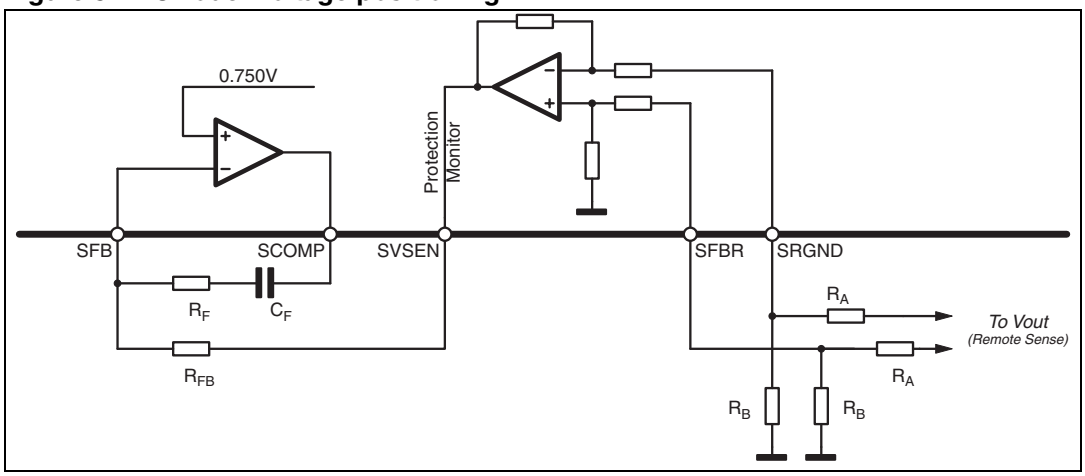
When enabled, single-phase is an independent regulator with 0.75 V fixed reference (load-line disabled - TM can be used as enable for the single-phase).

Output voltage higher than the internal reference may be achieved by adding a proper resistor divider (RA, RB - see *Figure 5*). To maintain precision in output voltage regulation, it is recommended to provide both SFBR and SRGND with the same divider.

Equation 1

$$V_{OUT} = 0.750V \cdot \frac{RA + RB}{RB}$$

Figure 5. JMode: voltage positioning



4.2 Programming HiZ level

The L6759D is able to manage different levels for HiZ on PWMx guaranteeing flexibility in driving different external drivers as well as DrMOS ICs.

Once VCC5, VDRV, and VIN voltages are above the respective UVLO (undervoltage lockout) thresholds (see *Figure 6*), the device uses PWM1 and PWM2 to detect the driver/DrMOS connected in order to program the suitable Hiz level of PWMx signals. During regulation, the Hiz level is used to force the external MOSFETs into high impedance state.

- PWM1 sources a constant 10 µA current, if its voltage results higher than 2.8 V, the HiZ level used during the regulation is 1.4 V, if lower, PWM2 information is used.
- PWM2 is kept in HiZ, if its voltage results higher than 2 V, the HiZ level used during the regulation is 2 V, if lower, 1.6 V.

An external resistor divider can be placed on PWM1 and PWM2 to force the detection of the correct HiZ level. They must be designed considering the external driver/DrMOS selected and the HiZ level requested.

Table 6. Pin-strapping (1)

Rdown [kΩ]	Rup [kΩ]	IMAX			ADDR				
		IMAX [A] (2)	JMode	VBOOT	SVI ADDR (3)	VFDE	DPM12	DPM23	Droop core
10	1.5	N · 25 + 56	ON	1.500 V	0100b	OFF	12 A	24 A	ON
10	2.7			1.350 V					OFF
22	6.8		OFF	1.500 V			10 A	20 A	ON
10	3.6			1.350 V					OFF
27	11	N · 25 + 48	ON	1.500 V			8 A	18 A	ON
12	5.6			1.350 V					OFF
82	43		OFF	1.500 V			OFF	OFF	ON
13	7.5			1.350 V					OFF
56	36	N · 25 + 40	ON	1.500 V		ON	12 A	24 A	ON
18	13			1.350 V					OFF
15	12		OFF	1.500 V			10 A	20 A	ON
18	16			1.350 V					OFF
15	14.7	N · 25 + 32	ON	1.500 V			8 A	18 A	ON
10	11			1.350 V					OFF
18	22		OFF	1.500 V			OFF	OFF	ON
56	75			1.350 V					OFF

Table 6. Pin-strapping (1) (continued)

Rdown [kΩ]	Rup [kΩ]	IMAX			ADDR				
		IMAX [A] (2)	JMode	VBOOT	SVI ADDR (3)	VFDE	DPM12	DPM23	Droop core
10	15	N · 25 + 24	ON	1.500 V	0010b	OFF	12 A	24 A	ON
12	20			1.350 V					OFF
12	22.6		OFF	1.500 V			10 A	20 A	ON
39	82			1.350 V					OFF
47	110	N · 25 + 16	ON	1.500 V			8 A	18 A	ON
10	27			1.350 V					OFF
22	68		OFF	1.500 V			OFF (4)	OFF (5)	ON
10	36			1.350 V					OFF
18	75	N · 25 + 8	ON	1.500 V		ON	12 A	24 A	ON
15	75			1.350 V					OFF
10	59		OFF	1.500 V			10 A	20 A	ON
10	75			1.350 V					OFF
10	100	N · 25	ON	1.500 V			8 A	18 A	ON
10	150			1.350 V					OFF
10	220		OFF	1.500 V			OFF (4)	OFF (5)	ON
10	Open			1.350 V					OFF

1. Suggested values, divider needs to be connected between VCC5 pin and GND.
2. N is the number of phase programmed for the multi-phase section.
3. Address for multi-phase. Single-phase not accessible.
4. Transition between 1Phase and 2Phase operation is set to 12 A but disabled in PS00h (minimum phase number in PS00h is 2).
5. Dynamic phase management disabled, IC always working at maximum possible number of phases except when in >PS00h when transitioning between 1Phase and 2Phase at 12 A.

Table 7. PMBus address definition

SVI address (see *Table 6*)	COMP to GND	PMBus address
0100b	4.99 k	EEh
	14.99 k	EAh
	24.99 k	E6h
	Open	E2h
0010b	4.99 k	ECh
	14.99 k	E8h
	24.99 k	E4h
	Open	E0h

5 Device description and operation

The L6759D is a programmable 2/3-phase PWM controller that provides complete control logic and protection to realize a high performance step-down DC-DC voltage regulator optimized for advanced DDR memory power supply. The device features 2nd generation LTB Technology™: through a load transient detector, it is able to turn on simultaneously all the phases. This allows the output voltage deviation to be minimized and, in turn, to minimize system costs by providing the fastest response to a load transition.

The L6759D implements current reading across the inductor in fully differential mode. A sense resistor in series to the inductor can be also considered to improve reading precision. The current information read corrects the PWM output in order to equalize the average current carried by each phase.

The controller supports VR12 specifications featuring 25 MHz SVI bus and all the required registers. The platform may program the defaults for these registers through dedicated pin-strapping.

A complete set of protection is available: overvoltage, undervoltage, overcurrent (per-phase and total) and feedback disconnection guarantee the load to be safe under all conditions.

Special power management features like DPM, VFDE and GDC modify the phase number, gate driving voltage and switching frequency to optimize the efficiency over the load range.

The L6759D is available in VFQFPN48 with a 6x6 mm body package.

5.1 Device initialization

Figure 6. Device initialization: default

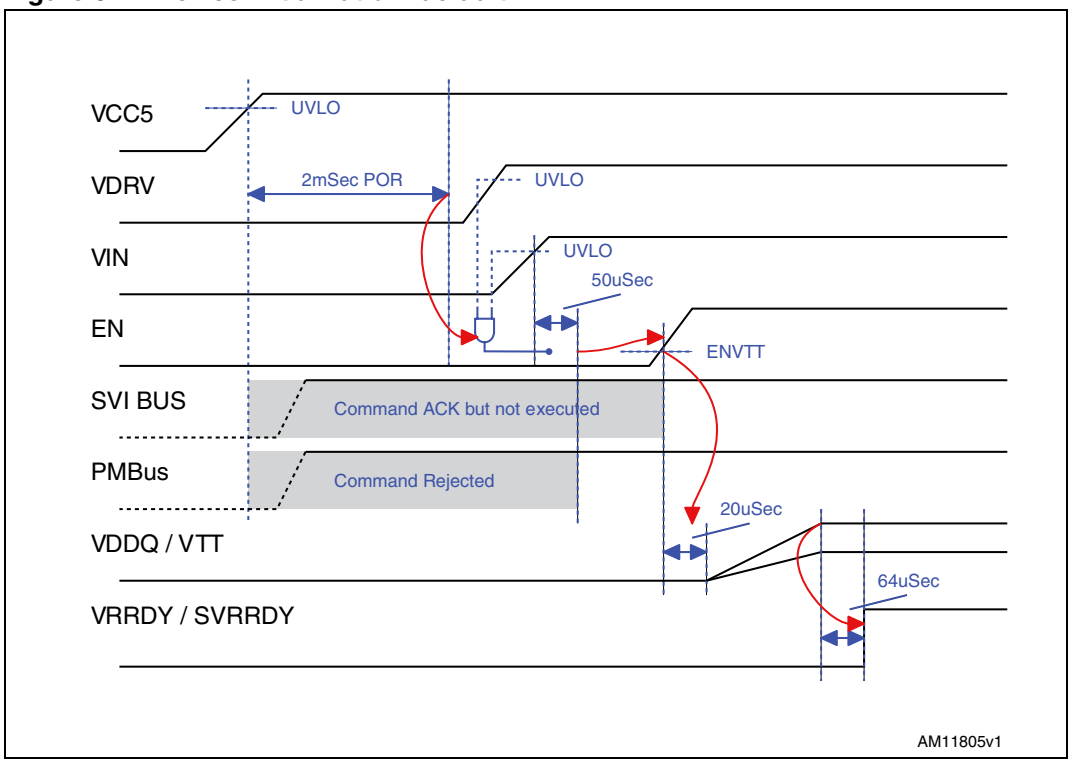
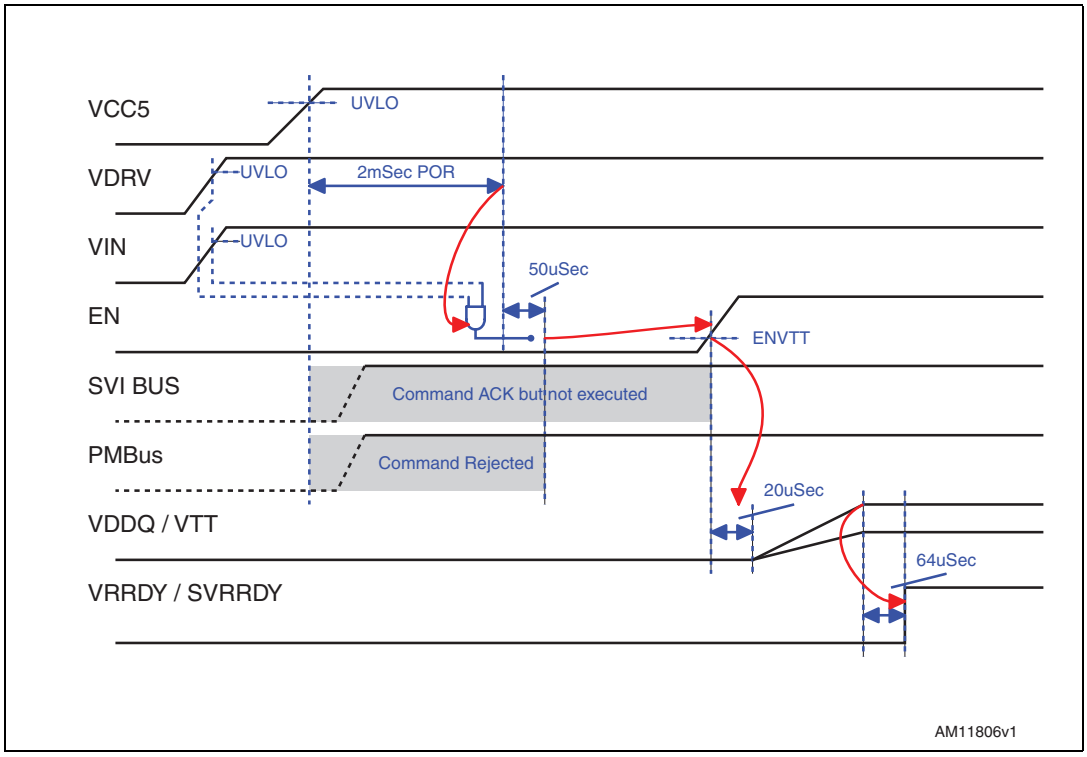


Figure 7. Device initialization: alternative sequence

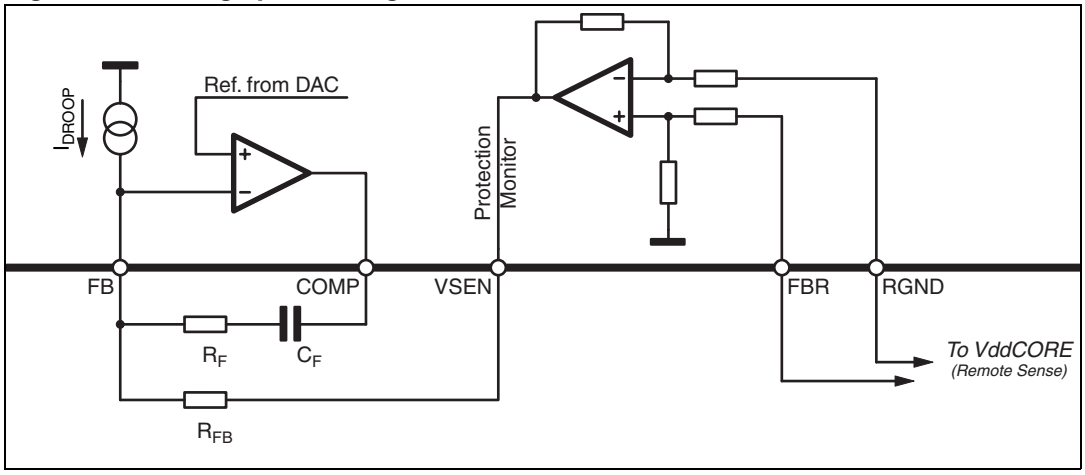


6 Output voltage positioning

Output voltage positioning is performed by selecting the controller operative-mode for the two sections and by programming the droop function effect (see *Figure 8*). The controller reads the current delivered by each section by monitoring the voltage drop across the DCR inductors. The current (I_{DROOP} / I_{SDROOP}) sourced from the FB / SFB pins, directly proportional to the read current, causes the related section output voltage to vary according to the external R_{FB} / R_{SFB} resistor, so implementing the desired load-line effect.

The L6759D embeds a dual remote-sense buffer to sense remotely the regulated voltage of each section without any additional external components. In this way, the output voltage programmed is regulated, compensating for board and socket losses. Keeping the sense traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

Figure 8. Voltage positioning



6.1 Multi-phase section - phase # programming

The multi-phase section implements a flexible 2 to 3 interleaved-phase converter. To program the desired number of phases, pull up with a 1 kΩ resistor to VCC5 the PWMx signal that is not required to be used.

Caution: For the disabled phase(s), the current reading pins need to be properly connected to avoid errors in current-sharing and voltage-positioning: CSxP needs to be connected to the regulated output voltage while CSxN needs to be connected to CSxP through the same R_G resistor used for the active phases. See *Figure 2* for details on 2-phase connections.

6.2 Multi-phase section - current reading and current sharing loop

The L6759D embeds a flexible, fully-differential current sense circuitry that is able to read across inductor parasitic resistance or across a sense resistor placed in series to the inductor element. The fully-differential current reading rejects noise and allows the placing of the sensing element in different locations without affecting the measurement's accuracy. The

trans-conductance ratio is issued by the external resistor R_G placed outside the chip between the CSxN pin toward the reading points. The current sense circuit always tracks the current information, the CSxP pin is used as a reference keeping the CSxN pin to this voltage. To correctly reproduce the inductor current, an R-C filtering network must be introduced in parallel to the sensing element. The current that flows from the CSxN pin is then given by the following equation (see *Figure 9*):

Equation 2

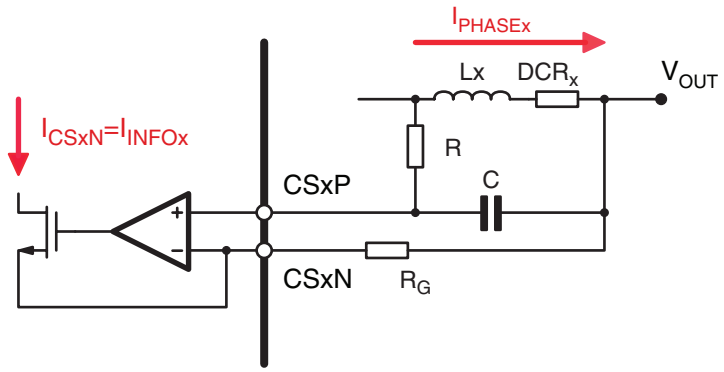
$$I_{CSxN} = \frac{DCR}{R_G} \cdot \frac{1 + s \cdot L/DCR}{1 + s \cdot R \cdot C} \cdot I_{PHASEx}$$

Considering the matching of the time constant between the inductor and the R-C filter applied (time constant mismatches cause the introduction of poles into the current reading network causing instability. In addition, it is also important for the load transient response and to let the system show resistive equivalent output impedance) it results:

Equation 3

$$\frac{L}{DCR} = R \cdot C \quad \Rightarrow \quad I_{CSxN} = \frac{R_L}{R_G} \cdot I_{PHASEx} = I_{INFOx}$$

Figure 9. Current reading



The current read through the CSxP / CSxN pairs is converted into a current I_{INFOx} proportional to the current delivered by each phase and the information about the average current $I_{AVG} = \Sigma I_{INFOx} / N$ is internally built into the device (N is the number of working phases). The error between the read current I_{INFOx} and the reference I_{AVG} is then converted into a voltage that, with a proper gain, is used to adjust the duty cycle whose dominant value is set by the voltage error amplifier in order to equalize the current carried by each phase.

6.3 Multi-phase section - defining load-line

The L6759D introduces a dependence of the output voltage on the load current recovering part of the drop due to the output capacitor ESR in the load transient. Introducing a dependence of the output voltage on the load current, a static error, proportional to the output current, causes the output voltage to vary according to the sensed current.

Figure 9 shows the current sense circuit used to implement the load-line. The current flowing across the inductor(s) is read through the R-C filter across the CSxP and CSxN pins. R_G programs a trans-conductance gain and generates a current I_{CSx} proportional to the current of the phase. The sum of the I_{CSx} current, with proper gain eventually adjusted by the PMBus commands, is then sourced by the FB pin (I_{DROOP}). R_{FB} gives the final gain to program the desired load-line slope (*Figure 8*).

Time constant matching between the inductor (L / DCR) and the current reading filter (RC) is required to implement a real equivalent output impedance of the system, so voiding over and/or undershoot of the output voltage as a consequence of a load transient. The output voltage characteristic vs. load current is then given by:

Equation 4

$$V_{OUT} = VID - R_{FB} \cdot I_{DROOP} = VID - R_{FB} \cdot \frac{DCR}{R_G} \cdot I_{OUT} = VID - R_{LL} \cdot I_{OUT}$$

where R_{LL} is the resulting load-line resistance implemented by the multi-phase section.

The R_{FB} resistor can be then designed according to the R_{LL} specifications as follows:

Equation 5

$$R_{FB} = R_{LL} \cdot \frac{R_G}{DCR}$$

6.4 Multi-phase section - IMON information

The voltage on the IMON pin contains the analog information related to the current delivered by the VR and it is digitized for VR12 current reporting. The pin sources a copy of the droop current:

Equation 6

$$I_{IMON} = I_{DROOP} = \frac{DCR}{R_G} \cdot I_{OUT}$$

See *Section 6* for details about current reading.

The Iout register contains analog-to-digital conversion of the voltage present on the IMON pin considering the following relationships:

a) $V_{IMON} = I_{IMON} \cdot R_{IMON}$ where R_{IMON} is the resistor connected between IMON and GND.

b) V_{IMON}=1.24 V corresponds to IMAX. R_{IMON} is designed according to this relationship.

Note: Current reporting precision may be affected by external layout. The internal ADC is referenced to the device GND pin: in order to perform the highest accuracy in the current monitor, R_{IMON} must be routed to the GND pin with a dedicated net to avoid GND plane drops affecting the precision of the measurement.

6.5 Single-phase section - disable

The single-phase section can be disabled by pulling high the SPWM pin. The related command is rejected.

6.6 Single-phase section - current reading

The single-phase section performs the same differential current reading across DCR as the multi-phase section. According to *Section 6.2*, the current that flows from the SCSN pin is then given by the following equation (see *Figure 9*):

Equation 7

$$I_{SCSN} = \frac{DCR}{R_{SG}} \cdot I_{SOUT} = I_{SDROOP}$$

6.7 Single-phase section - defining load-line

This method introduces a dependence of the output voltage on the load current recovering part of the drop due to the output capacitor ESR in the load transient. Introducing a dependence of the output voltage on the load current, a static error, proportional to the output current, causes the output voltage to vary according to the sensed current.

Figure 9 shows the current sense circuit used to implement the load-line. The current flowing across the inductor DCR is read through R_{SG}. R_{SG} programs a trans-conductance gain and generates a current I_{SDROOP} proportional to the current delivered by the single-phase section that is then sourced from the SFB pin with proper gain eventually adjusted by the PMBus commands. R_{SFB} gives the final gain to program the desired load-line slope (*Figure 8*).

The output characteristic vs. load current is then given by:

Equation 8

$$V_{SOUT} = VID - R_{SFB} \cdot I_{SDROOP} = = VID - R_{SFB} \cdot \frac{DCR}{R_{SG}} \cdot I_{SOUT} = VID - R_{SLL} \cdot I_{SOUT}$$

where R_{SLL} is the resulting load-line resistance implemented by the single-phase section.

The R_{SFB} resistor can be then designed according to R_{SLL} as follows:

Equation 9

$$R_{SFB} = R_{SLL} \cdot \frac{R_{SG}}{DCR}$$

6.8 Dynamic VID transition support

The L6759D manages dynamic VID transitions that allow the output voltage of both sections to modify during normal device operation for power management purposes. OV, UV, and per-phase OC signals are masked during every DVID transition and they are re-activated with proper delay to prevent false triggering. Total OC is active even during DVID.

When dynamically changing the regulated voltage (DVID), the system needs to charge or discharge the output capacitor accordingly. This means that an extra-current I_{DVID} needs to be delivered (especially when increasing the output regulated voltage) and it must be considered when setting the overcurrent threshold of both the sections. This current results:

Equation 10

$$I_{DVID} = C_{OUT} \cdot \frac{dV_{OUT}}{dT_{VID}}$$

where dV_{OUT} / dT_{VID} depends on the specific command issued (10 mV/µsec. for SetVID_Fast and 2.5 mV/µsec. for SetVID_Slow). Surpassing the total OC threshold during the dynamic VID causes the device to latch and disable. Set proper filtering on I_{LIM} to prevent from false total-OC tripping.

As soon as the controller receives a new valid command to set the VID level for one (or both) of the two sections, the reference of the involved section steps up or down according to the target VID with the programmed slope until the new code is reached. If a new valid command is issued during the transition, the device updates the target-VID level and performs the dynamic transition up to the new code. OV and UV are masked during the transition and re-activated with proper delay after the end of the transition to prevent false triggering.

6.9 DVID optimization: REF

A high slew-rate for dynamic VID transitions cause overshoot and undershoot on the regulated voltage, causing a violation in the microprocessor requirement. To compensate for this behavior and to remove any undershoot in the transition, each section features a DVID optimization circuit.

The reference used for the regulation is available on the REF/SREF pin (see *Figure 10*). Connect an R_{REF}/C_{REF} to GND to optimize the DVID behavior. The components may be designed as follows:

Equation 11

$$C_{REF} = C_F \cdot \left(1 - \frac{\Delta V_{OSC}}{k_V \cdot V_{IN}}\right)$$

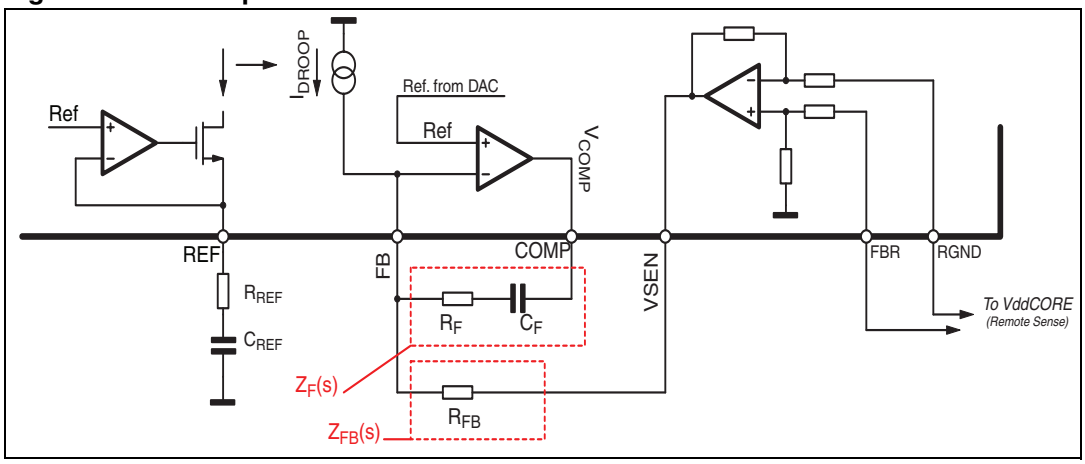
$$R_{REF} = \frac{R_F \cdot C_F}{C_{REF}}$$

where ΔVosc is the PWM ramp and k_V the gain for the voltage loop (see *Section 11*).

During a DVID transition, the REF pin moves according to the command issued (SetVIDFast, SetVIDSlow); the current requested to charge/discharge the R_{REF}/C_{REF} network is mirrored and added to the droop current compensating for undershoot on the regulated voltage.

Optimization through the REF pin is active only for downward VID transition.

Figure 10. DVID optimization circuit



7 Output voltage monitoring and protection

The L6759D monitors the regulated voltage of both sections through pin VSEN and SVSEN in order to manage OV and UV. The device shows different thresholds when in different operative conditions but the behavior in response to a protection event is still the same as described below.

Protection is active also during soft-start while it is properly masked during DVID transitions with an additional delay to avoid false triggering.

Table 8. L6759D protection at a glance

	Section	
	Multi-phase	**Single-phase**
Overvoltage (OV)	VSEN, SVSEN = +150 mV above reference. ***Action:*** IC latch; LS=ON & PWMx = 0 (if applicable); other section: HiZ.	
Undervoltage (UV)	VSEN, SVSEN = 400 mV below reference. Active after Ref > 500 mV ***Action:*** IC latch; both sections HiZ.	
Overcurrent (OC)	Current monitor across inductor DCR. Dual protection, per-phase and average. ***Action:*** UV-like	
Dynamic VID	Protection masked with additional delay to prevent from false triggering.	n/a

7.1 Overvoltage

When the voltage sensed by VSEN and/or SVSEN overcomes the OV threshold, the controller acts in order to protect the load from excessive voltage levels, avoiding any possible undershoot. To reach this target, a special sequence is performed as per the following list:

- The reference performs a DVID transition down to 250 mV on the section which triggered the OV protection
- The PWM of the section which triggered the protection are switched between HiZ and zero (ENDRV is kept high) in order to follow the voltage imposed by the DVID on-going. This limits the output voltage excursion, protects the load and assures no undershoot is generated (if Vout < 250 mV, the section is HiZ)
- The PWM of the non-involved section is set permanently to HiZ (ENDRV is kept low) in order to realize a HiZ condition
- OSC/ FLT pin is driven high
- Power supply or EN pin cycling is required to restart operations
- If the cause of the failure is removed, the converter ends the transition with all PWMs in HiZ state and the output voltage of the section which triggered the protection lower than 250 mV.

7.2 Overcurrent

The overcurrent threshold must be programmed to a safe value, in order to be sure that each section doesn't enter OC during normal operation of the device. This value must take

into consideration also the extra current needed during the DVID transition (I_{DVID}) and the process spread and temperature variations of the sensing elements (inductor DCR).

Moreover, since also the internal threshold spreads, the design must consider the minimum/maximum values of the threshold.

7.2.1 Multi-phase section

The L6759D features two independent load indicator signals, IMON and I_{LIM}, to properly manage OC protection, current monitoring and DPM. Both IMON and I_{LIM} sources a current proportional to the current delivered by the regulator, as follows:

Equation 12

$$I_{MON} = I_{LIM} = \frac{DCR}{R_G} \cdot I_{OUT}$$

The I_{MON} and I_{LIM} pins are connected to GND through a resistor (R_{IMON} and R_{ILIM} respectively), implementing a load indicator with different targets.

- IMON is used for current reporting purposes and for the DPM phase shedding. R_{IMON} must be designed considering that I_{MAX} must correspond to 1.24 V (for correct IMAX detection)
- I_{LIM} is used for the overcurrent protection only. R_{ILIM} must be designed considering that the OC protection is triggered when $V(I_{LIM})$=2.5 V.

In addition, the L6759D also performs per-phase OC protection.

- Per-phase OC. Maximum information current per-phase (I_{INFOx}) is internally limited to 35 µA. This end-of-scale current (I_{OC_TH}) is compared with the information current generated for each phase (I_{INFOx}). If the current information for the single-phase exceeds the end-of-scale current (i.e. if $I_{INFOx} > I_{OC_TH}$), the device turns on the LS MOSFET until the threshold is re-crossed (i.e. until $I_{INFOx} < I_{OC_TH}$)
- Total current OC. The I_{LIM} pin allows a maximum total output current to be defined for the system (I_{OC_TOT}). The I_{LIM} current is sourced from the I_{LIM} pin. By connecting a resistor R_{ILIM} to GND, a load indicator with 2.5 V (V_{OC_TOT}) end-of-scale can be implemented. When the voltage present at the I_{LIM} pin crosses V_{OC_TOT}, the device detects an OC and immediately latches with all the MOSFETs of all the sections OFF (HiZ).

The typical design considers the intervention of the total current OC before the per-phase OC, leaving this last one as an extreme-protection in case of hardware failures in the external components. Per-phase OC depends on the R_G design while total OC is dependant on the I_{LIM} design and on the application TDC and max. current supported. The typical design flow is the following:

- Define the maximum total output current (I_{OC_TOT}) according to system requirements (I_{MAX}, I_{TDC}). Considering the I_{MON} design, I_{MAX} must correspond to 1.24 V (for correct IMAX detection) while in the I_{LIM} design, I_{OC_TOT} must correspond to 2.5 V
- Design the per-phase OC and R_G resistor in order to have $I_{INFOx} = I_{OC_TH}$ (35 µA) when I_{OUT} is about 10% higher than the I_{OC_TOT} current. It results:

Equation 13

$$R_G = \frac{(1.1 \cdot I_{OC_TOT}) \cdot DCR}{N \cdot I_{OCTH}}$$

where N is the number of phases and DCR the DC resistance of the inductors. R_G should be designed in worst-case conditions

- Design the R_{IMON} in order to have the IMON pin voltage to 1.24 V at the I_{MAX} current specified by the design. It results:

Equation 14

$$R_{IMON} = \frac{1.24V \cdot R_G}{I_{MAX} \cdot DCR}$$

where I_{MAX} is max. current requested by the processor (see Intel documentation for details)

- Design the R_{ILIM} in order to have the I_{LIM} pin voltage to 2.5 V at the I_{OC_TOT} current specified above. It results:

Equation 15

$$R_{ILIM} = \frac{2.5V \cdot R_G}{I_{OC_TOT} \cdot DCR}$$

where I_{OC_TOT} is the overcurrent switch-over threshold previously defined

- Adjust the defined values according to the bench-test of the application
- C_{ILIM} in parallel to R_{ILIM} can be added with a proper time constant to prevent false OC tripping and/or delay
- C_{IMON} in parallel to R_{IMON} can be added to adjust the averaging interval for the current reporting and/or to adjust the DPM latencies. Additionally, it can be increased to prevent false Total-OC tripping during DVID.

Note: This is the typical design flow. Custom design and specifications may require different settings and ratios between the per-phase OC threshold and the total current OC threshold. Applications with big ripple across inductors may be required to set per-phase OC to values different than 110%: the design flow should be modified accordingly.

7.2.2 Overcurrent and power states

When the controller receives the SetPS command through the SVI interface, it automatically changes the number of working phases. In particular, the maximum number of phases in which L6759D may work in > PS00h is limited to 2, regardless of the number N configured in PS00h.

The OC level is then scaled as the controller enters > PS00h, as per *Table 9*.

Table 9. Multi-phase section OC scaling and power states

Power state [Hex]	N	OC level (V_{OC_TOT})
00h	2 to 3	2.500 V

Table 9. Multi-phase section OC scaling and power states (continued)

Power state [Hex]	N	OC level (V_{OC_TOT})
01h, 02h	3	1.650 V
	2	2.500 V

7.2.3 Single-phase section

The L6759D monitors both the per-phase currents and allows the setting of an OC threshold as follows:

- Per-phase OC. Maximum information current per-phase (I_{SINFOx}) is internally limited to 35 µA. This end-of-scale current (I_{SOC_TH}) is compared with the information current generated for each phase (I_{SINFOx}). If the current information for the single-phase exceeds the end-of-scale current (i.e. if $I_{SINFOx} > I_{SOC_TH}$), the device turns on the LS MOSFET until the threshold is re-crossed (i.e. until $I_{SINFOx} < I_{SOC_TH}$).

  Typical design is dependant on the application TDC and max. current supported. The typical design flow is the following:

  – Define the maximum total output current (I_{SOC_TOT}) according to system requirements (I_{SMAX}, I_{STDC}).
  – Design the per-phase OC and R_{SG} resistor in order to have $I_{SINFOx} = I_{SOC_TH}$ (35 µA) when $I_{SOUT} = I_{SOC_TOT}$ current. It results:

Equation 16

$$R_{SG} = \frac{I_{SOC_TOT} \cdot DCR}{I_{SOCTH}}$$

where DCR is the DC resistance of the inductors. R_{SG} should be designed in worst-case conditions.

  – Adjust the defined values according to the bench-test of the application.

8 Single NTC thermal monitor and compensation

The L6759D features single NTC for thermal sensing for both thermal monitoring and compensation. Thermal monitoring consists of monitoring the converter temperature eventually reporting an alarm by asserting the VR_HOT signal. This is the base for the temperature zone register fill. Thermal compensation consists of compensating the inductor DCR derating with temperature, so preventing drifts in any variable correlated to the DCR: voltage positioning, overcurrent, Imon, current reporting. Both functions share the same thermal sensor (NTC) to optimize the overall application cost without compromising performance.

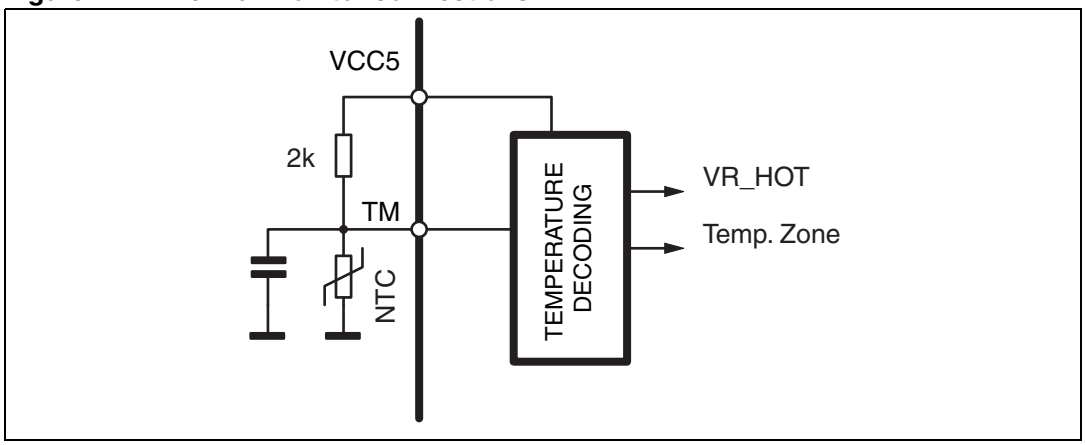
8.1 Thermal monitor and VR_HOT

The diagram for the thermal monitor is reported in *Figure 11*. NTC should be placed close to the power stage hot-spot in order to sense the regulator temperature. As the temperature of the power stage increases, the NTC resistive value decreases, so reducing the voltage observable at the TM pin.

The recommended NTC is NTHS0805N02N6801HE for accurate temperature sensing and thermal compensation. Different NTC may be used: to reach the requested accuracy in temperature reporting, a proper resistive network must be used in order to match the resulting characteristic with the one coming from the recommended NTC.

The voltage observed at the TM pin is internally converted and then used to fill in the temperature zone register. When the temperature observed exceeds TMAX (programmed via PMBus, the default value is 110 °C), the L6759D asserts VR_HOT (active low - as long as the overtemperature event lasts) and the ALERT# line (until reset by the GetReg command on the status register).

Figure 11. Thermal monitor connections



8.2 Thermal compensation

The L6759D supports DCR sensing for output voltage positioning: the same current information used for voltage positioning is used to define the overcurrent protection and the current reporting (Register 15h in SVI). Having imprecise and temperature-dependant information leads to a violation of the specifications and misleading information returned to the SVI master: a positive thermal coefficient specific to DCR needs to be compensated to get stable behavior of the converter as the temperature increase. Un-compensated systems show temperature dependencies on the regulated voltage, overcurrent protection and current reporting (Reg 15h).

The temperature information available on the TM pin and used for the thermal monitor may be used also for this purpose. By comparing the voltage on the TM pin with the voltage present on the TCOMP pin, the L6759D gives a correction to the I_{DROOP} current used for voltage positioning (see *Section 6.3*) therefore recovering the DCR temperature deviation. Depending on NTC location and distance from the inductors and the available airflow, the correlation between NTC temperature and DCR temperature may be different: TCOMP adjustments allow modification of the gain between the sensed temperature and the correction made upon the I_{DROOP} current.

Short TCOMP to GND to disable thermal compensation (no correction is given to I_{DROOP}).

8.3 TM and TCOMP design

This procedure applies to both single-phase and multi-phase sections.

1. Properly choose the resistive network to be connected to the TM pin. The recommended values/network is reported in *Figure 11*
2. Connect the voltage generator to the TCOMP pin (default value 3.3 V)
3. Power on the converter and load the thermal design current (TDC) with the desired cooling conditions. Record the output voltage regulated as soon as the load is applied
4. Wait for thermal steady-state. Adjust down the voltage generator on the TCOMP pin in order to get the same output voltage recorded at point #3
5. Design the voltage divider connected to TCOMP (between VCC5 and GND) in order to get the same voltage set to TCOMP at point #4
6. Repeat the test with the TCOMP divider designed at point #5 and verify the thermal drift is acceptable. In case of positive drift (i.e. output voltage at thermal steady-state is bigger than the output voltage immediately after loading TDC current), change the divider at the TCOMP pin in order to reduce the TCOMP voltage. In case of negative drift (i.e. output voltage at thermal steady-state is smaller than the output voltage immediately after loading TDC current) change the divider at the TCOMP pin in order to increase the TCOMP voltage
7. The same procedure can be implemented with a variable resistor in place of one of the resistors of the divider. In this case, once the compensated configuration is found, simply replace the variable resistor with a resistor with the same value.

9 Efficiency optimization

As per VR12 specifications, the SVI master may define different power states for the VR controller. This is performed by SetPS commands. The L6759D re-configures itself to improve overall system efficiency according to *Table 10*.

Table 10. Efficiency optimization

Feature	PS00h	PS01h
DPM	According to pin-strapping and PMBus(TM).	Active. 1Phase/2Phase according to Iout.
VFDE	Active when in single-phase and DPM enabled.	Active when in single-phase
GDC	According to pin-strapping and PMBus(TM).	GDC set to 5 V.

9.1 Dynamic phase management (DPM)

Dynamic phase management allows the number of working phases to be adjusted according to the delivered current still maintaining the benefits of the multi-phase regulation.

The phase number is reduced by monitoring the voltage level across the IMON pin: the L6759D reduces the number of working phases according to the strategy defined by the pin-strapping configured and/or PMBus(TM) commands received (see *Table 6*). DPM12 refers to the current at which the controller changes from 1 to 2 phases while DPM23 defines the current at which the controller changes from 2 to 3 phases.

When DPM is enabled, the L6759D starts monitoring the IMON voltage for phase number modification after VR_RDY has transition high: the soft-start is then implemented in interleaving mode with all the available phases enabled.

DPM is reset in case of a SetVID command that affects the multi-phase section and when LTB Technology™ detects a load transient. After being reset, if the voltage across IMON is compatible, DPM is re-enabled after a proper delay.

Delay in the intervention of DPM can be adjusted by properly sizing the filer across the IMON pin. Increasing the capacitance results in increased delay in the DPM intervention.

Note: During load transients with light slope, the filtering of IMON may result too slow for the IC to set the correct number of phases required for the current effectively loading the system (LTB does not trigger in case of light slopes). The L6759D features a safety mechanism which re-enables phases that were switched off by comparing I_{LIM} and IMON pin voltage. In fact, the I_{LIM} pin is lightly filtered in order to perform a fast reaction of OC protection while IMON is heavily filtered to perform the correct averaging of the information. While working continuously in DPM, the device compares the information of IMON and I_{LIM}: I_{LIM} voltage is divided into N steps with a width of $V_{OCP}/(2*N)$ (where V_{OCP} = 2.5 V and N the number of stuffed phases). If the DPM phase number resulting from IMON is not coherent with the step in which I_{LIM} stays, the phase number is increased accordingly.The mechanism is active only to increase the phase number which is reduced again by DPM.

9.2 Variable frequency diode emulation (VFDE)

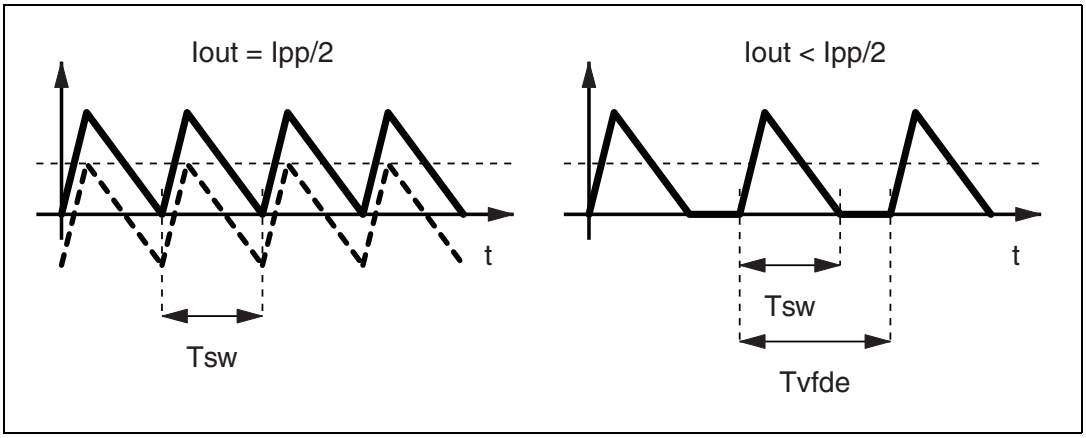
As the current required by the load is reduced, the L6759D progressively reduces the number of switching phases according to DPM settings on the multi-phase section. If single-phase operation is configured, when the delivered current approaches the CCM/DCM boundary, the controller enters VFDE operation. The single-phase section, being a single-phase, enters VFDE operation always when the delivered current approaches the CCM/DCM boundary.

In a common single-phase DC-DC converter, the boundary between CCM and DCM is when the delivered current is perfectly equal to 1/2 of the peak-to-peak ripple into the inductor (Iout = Ipp/2). Further decreasing the load in this condition maintaining CCM operation would cause the current into the inductor to reverse, therefore sinking current from the output for a part of the off-time. This results in poor system efficiency.

The L6759D is able (via CSPx/CSNx pins) to detect the sign of the current across the +inductor (zero cross detection, ZCD), so it is able to recognize when the delivered current approaches the CCM/DCM boundary. In VFDE operation, the controller fires the high-side MOSFET for a TON and the low-side MOSFET for a TOFF (the same as when the controller works in CCM mode) and waits for the necessary time until the next firing in high-impedance (HiZ). The consequence of this behavior is a linear reduction of the “apparent” switching frequency that, in turn, results in an improvement of the efficiency of the converter when in very light load conditions.

To prevent entering the audible range, the “apparent” switching frequency reduction is limited to 30 kHz.

Figure 12. Output current vs. switching frequency in PSK mode



9.3 Gate drive control (GDC)

Gate drive control (GDC) is a proprietary function which allows the L6759D to dynamically control the Power MOSFETs driving voltage in order to further optimize the overall system efficiency. According to the SVI power state commanded and the configuration received through the PMBus, the device switches this pin (GDC) between the VCC5 or VDRV (inputs). By connecting the power supply of external drivers directly to this pin, it is then possible to control carefully the external MOSFET driving voltage.

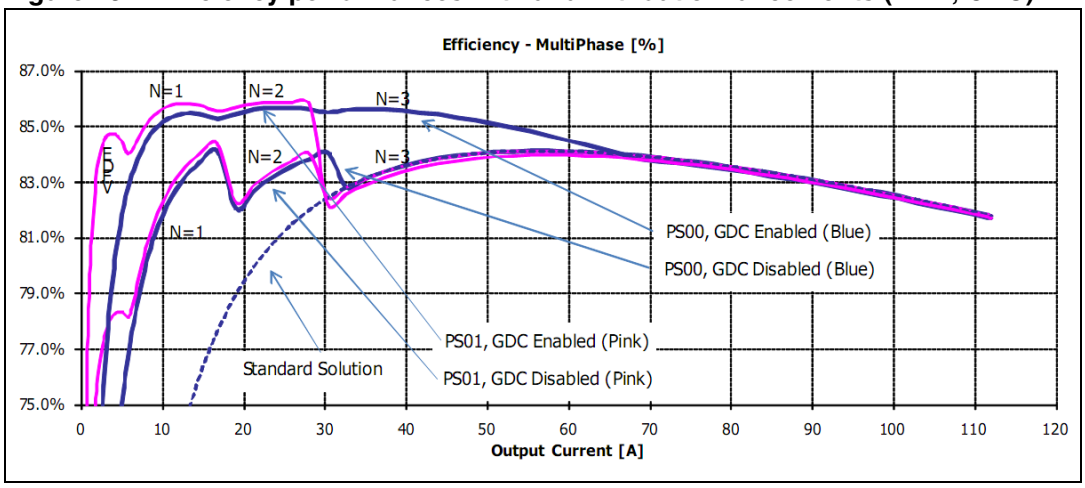
In fact, high driving voltages are required to get good efficiencies in high loading conditions. On the contrary, in lower loading conditions, such high driving voltage penalizes efficiency because of high losses in Qgs. GDC allows to tune the MOSFET driving voltage according to the delivered current.

Default configuration considers GDC always switched to VDRV except when the current monitor is lower than N*10 or when entering power states higher than PS01h (included): in this case, to further increase efficiency, simply supply the Phase1 and Phase2 driver through the GDC pin. Their driving voltage is automatically updated as lower power states are commanded through the SVI interface.

Further optimization may be possible by properly setting the automatic GDC threshold through a dedicated PMBus command. It is then possible to modify the gate driving voltage switch-over in PS00h. According to the positioning of the threshold compared with DPM thresholds, it is possible to achieve different performances. Simulations and/or bench tests may be of help in defining the best performing configuration achievable with the active and passive components available.

Figure 13 gives a comparison of the efficiency improvements with DPM/GDC enabled with respect to standard solutions.

Figure 13. Efficiency performances with and without enhancements (DPM, GDC)



10 Main oscillator

The internal oscillator generates the triangular waveform for the PWM charging and discharging an internal capacitor with a constant current. The switching frequency for each channel is internally fixed at 200 kHz (F_{SW}) and at 230 kHz (F_{SSW}): the resulting switching frequency at the load side for the multi-phase section results in being multiplied by N (number of configured phases).

The current delivered to the oscillator is typically 20 µA and may be varied using an external resistor (R_{OSC}, R_{SOSC}) typically connected between the OSC, SOSC pins and GND. Since the OSC/SOSC pins are fixed at 1.02 V, the frequency is varied proportionally to the current sunk from the pin considering the internal gain of 10 kHz/µA for the multi-phase section and of 11.5 kHz/µA for the single-phase section, see *Figure 14*.

By connecting R_{OSC}/R_{SOSC} to SGND the frequency is increased (current is sunk from the pin), according to the following relationships:

Equation 17

$$F_{SW} = 200\text{kHz} + \frac{1.02\text{V}}{R_{OSC}(\text{k}\Omega)} \cdot 10\frac{\text{kHz}}{\mu\text{A}}$$

Equation 18

$$F_{SSW} = 230\text{kHz} + \frac{1.02\text{V}}{R_{SOSC}(\text{k}\Omega)} \cdot 11.5\frac{\text{kHz}}{\mu\text{A}}$$

Connecting R_{OSC}/R_{SOSC} to a positive voltage Vbias, the frequency is reduced (current is injected into the pin), according to the following relationships:

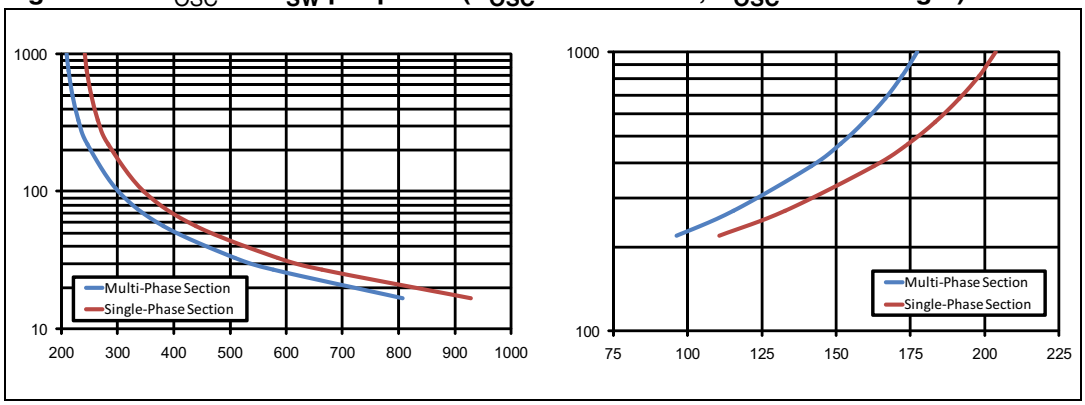
Equation 19

$$F_{SW} = 200\text{kHz} - \frac{\text{Vbias} - 1.02\text{V}}{R_{OSC}(\text{k}\Omega)} \cdot 10\frac{\text{kHz}}{\mu\text{A}}$$

Equation 20

$$F_{SSW} = 230\text{kHz} - \frac{\text{Vbias} - 1.02\text{V}}{R_{SOSC}(\text{k}\Omega)} \cdot 11.5\frac{\text{kHz}}{\mu\text{A}}$$

Figure 14. R_{OSC} vs. F_{SW} per phase (R_{OSC} to GND - left; R_{OSC} to 3.3V - right)



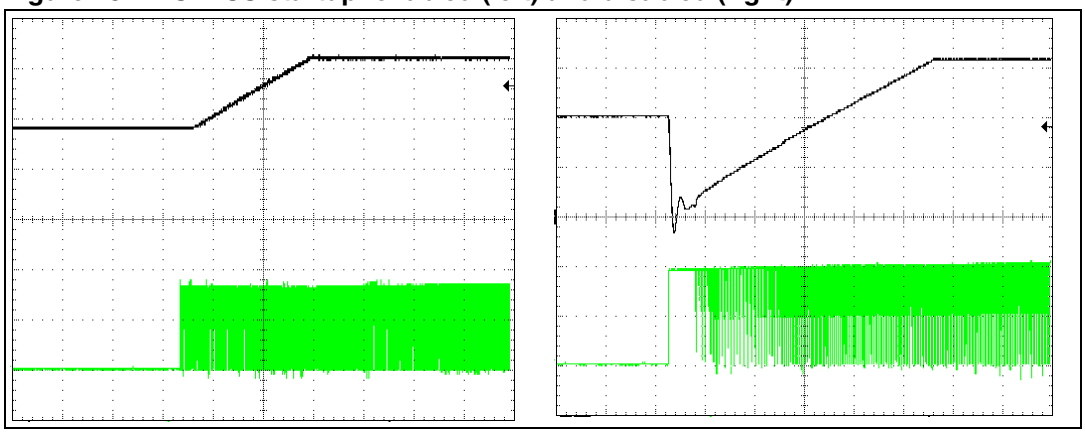
10.1 LSLESS startup and pre-bias output

Any time the device resumes from an “OFF” code and at the first power-up, in order to avoid any kind of negative undershoot on the load side, the L6759D performs a special sequence in enabling the drivers: during the soft-start phase, the LS driver results as disabled (LS=OFF - PWMx set to HiZ and ENDRV = 0) until the first PWM pulse. After the first PWM pulse, PWMx outputs switch between logic “0” and logic “1” and ENDRV is set to logic “1”.

This particular sequence avoids a dangerous negative spike on the output voltage that can happen if starting over a pre-biased output.

Low-side MOSFET turn-on is masked only from the control loop point of view: protections are still allowed to turn on the low-side MOSFET in the case of overvoltage if needed.

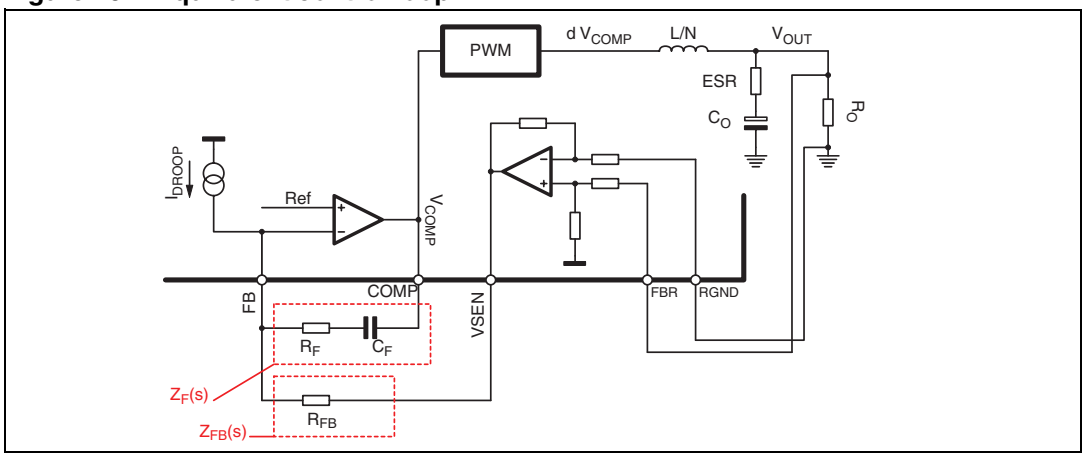
Figure 15. LSLESS startup: enabled (left) and disabled (right)



11 System control loop compensation

The control system can be modeled with an equivalent single-phase converter whose only difference is the equivalent inductor L/N (where each phase has an L inductor and N is the number of the configured phases), see *Figure 16*.

Figure 16. Equivalent control loop



The control loop gain results (obtained opening the loop after the COMP pin):

Equation 21

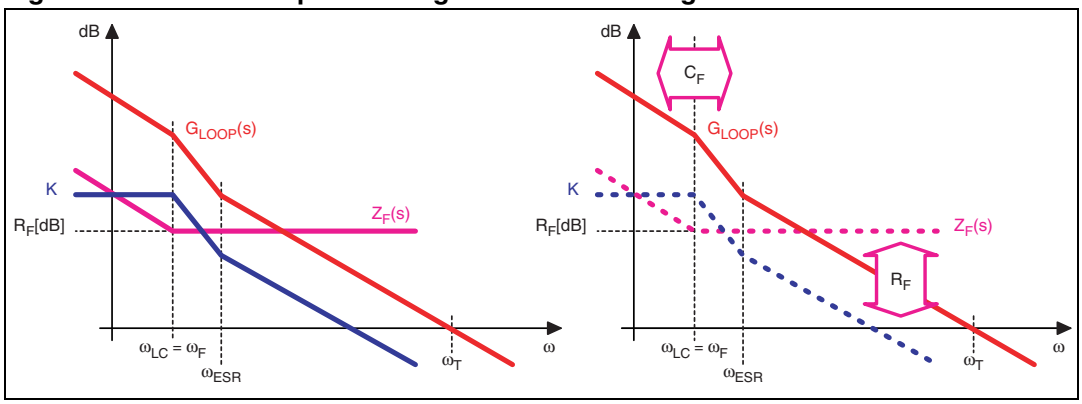
$$G_{LOOP}(s) = -\frac{PWM \cdot Z_F(s) \cdot (R_{LL} + Z_P(s))}{[Z_P(s) + Z_L(s)] \cdot \left[\frac{Z_F(s)}{A(s)} + \left(1 + \frac{1}{A(s)}\right) \cdot R_{FB}\right]}$$

where:

- R_{LL} is the equivalent output resistance determined by the droop function (voltage positioning)
- $Z_P(s)$ is the impedance resulting from the parallel of the output capacitor (and its ESR) and the applied load R_O
- $Z_F(s)$ is the compensation network impedance
- $Z_L(s)$ is the equivalent inductor impedance
- A(s) is the error amplifier gain
- $PWM = \frac{9}{10} \cdot \frac{V_{IN}}{\Delta V_{OSC}}$ is the PWM transfer function.

The control loop gain is designed in order to obtain a high DC gain to minimize static error and to cross the 0dB axes with a constant -20 dB/dec slope with the desired crossover frequency ω_T. Neglecting the effect of $Z_F(s)$, the transfer function has one zero and two poles; both the poles are fixed once the output filter is designed (LC filter resonance ω_{LC}) and the zero (ω_{ESR}) is fixed by ESR and the droop resistance.

Figure 17. Control loop Bode diagram and fine tuning



To obtain the desired shape, an R_F-C_F series network is considered for the $Z_F(s)$ implementation. A zero at $\omega_F=1/R_FC_F$ is then introduced together with an integrator. This integrator minimizes the static error while placing the zero ω_F in correspondence with the L-C resonance which assures a simple -20 dB/dec shape of the gain.

In fact, considering the usual value for the output filter, the LC resonance results to be at a frequency lower than the above reported zero.

The compensation network can be designed as follows:

Equation 22

$$R_F = \frac{R_{FB} \cdot \Delta V_{OSC}}{V_{IN}} \cdot \frac{10}{6} \cdot \frac{F_{SW} \cdot L}{(R_{LL} + ESR)}$$

Equation 23

$$C_F = \frac{\sqrt{C_O \cdot L}}{R_F}$$

11.1 Compensation network guidelines

The compensation network design assures the presence of a system response according to the crossover frequency selected and to the output filter considered: it is anyway possible to further fine-tune the compensation network modifying the bandwidth in order to get the best response of the system, as follows (see *Figure 17*):

- Increase R_F to increase the system bandwidth accordingly
- Decrease R_F to decrease the system bandwidth accordingly
- Increase C_F to move ω_F to low frequencies increasing as a consequence the system phase margin.

Having the fastest compensation network does not guarantee that the load requirements are satisfied: the inductor still limits the maximum dI/dt that the system can afford. In fact, when a load transient is applied, the best that the controller can do is to “saturate” the duty cycle to its maximum (d_{MAX}) or minimum (0) value. The output voltage dV/dt is then limited by the inductor charge / discharge time and by the output capacitance. In particular, the most

limiting transition corresponds to the load-removal since the inductor results as being discharged only by Vout (while it is charged by V_{IN}-V_{OUT} during a load appliance).

Note: The introduction of a capacitor (C_I) in parallel to R_{FB} significantly speeds up the transient response by coupling the output voltage dV/dt on the FB pin, therefore using the error amplifier as a comparator. The COMP pin suddenly reacts and, also thanks to the LTB Technology™ control scheme, all the phases can be turned on together to immediately give to the output the required energy. Typical design considers starting from values in the range of 100 pF validating the effect by bench testing. An additional series resistor (R_I) can also be used.

11.2 LTB Technology

LTB Technology further enhances the performance of the controller by reducing the system latencies and immediately turning on all the phases to provide the correct amount of energy to the load optimizing the output capacitor count.

LTB Technology monitors the output voltage through a dedicated pin detecting load-transients with selected dV/dt, it cancels the interleaved phase-shift, simultaneously turning on all phases.

The LTB detector is able to detect output load transients by coupling the output voltage through an R_{LTB} - C_{LTB} network. After detecting a load transient, all the phases are turned on together and the EA latencies results as bypassed as well.

Sensitivity of the load transient detector can be programmed in order to control precisely both the undershoot and the ring-back.

LTB Technology design tips.

- Decrease R_{LTB} to increase the system sensitivity making the system sensitive to smaller dV_{OUT}
- Increase C_{LTB} to increase the system sensitivity making the system sensitive to higher dV/dt
- Increase R_i to increase the width of the LTB pulse
- Increase C_i to increase the LTB sensitivity over frequency.

12 PMBus support

The L6759D is compatible with PMBus™ standard revision 1.1, refer to PMBus standard documentation for further information (www.pmbus.org).

Table 11. Supported commands

Command	Per rail	Code [Hex]	Mode	Comments
OPERATION	Y	01	RW byte	Used to turn the controller on/off in conjunction with the input from the control pin. Also used to set margin voltages. Soft-off not supported
ON_OFF_CONFIG	N*1*	02	RW byte	Configures how the controller responds when power is applied.
WRITE_PROTECT	Y	10	RW byte	Controls writing to the PMBus device to prevent accidental changes.
VOUT_COMMAND	Y	21	RW word	Causes the converter to set it's output voltage to the commanded value - VID mode.
VOUT_MAX	Y	24	RW word	Sets the upper limit on the output voltage regardless of any other command
VOUT_MARGIN_HIGH	Y	25	RW word	Sets the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”
VOUT_MARGIN_LOW	Y	26	RW word	Sets the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”
IOUT_CAL_OFFSET	Y	39	RW word	Calibration for IOUT reading.
OT_FAULT_LIMIT	Y	4F	RW word	Overtemperature fault threshold.
OT_WARN_LIMIT	Y	51	RW word	Overtemperature warning threshold.
VIN_OV_FAULT_LIMIT	N	55	RW word	Input voltage monitor overvoltage limit.
VIN_UV_FAULT_LIMIT	N	59	RW word	Input voltage monitor undervoltage limit.
MFR_SPECIFIC_01	N	D1	RW byte	AVERAGE_TIME_SCALE. Sets the time between two measures.
MFR_SPECIFIC_02	Y	D2	RW byte	DEBUG_MODE. [01/10] Switch [ON/OFF] the Vout control on PMBus domain.
MFR_SPECIFIC_05	Y	D5	RW byte	VOUT_TRIM. Used to apply a fixed offset voltage to the output voltage command value.
MFR_SPECIFIC_08	Y	D8	RW byte	VOUT_DROOP. Used to change the Vout droop.
MFR_SPECIFIC_35	N*1*	F3	RW byte	MANUAL_PHASE_SHEDDING. Used to manage the phase shedding manually.
MFR_SPECIFIC_38	Y	F6	RW byte	VOUT_OV_FAULT_LIMIT allows the programming of the OV protection threshold for each rail.
MFR_SPECIFIC_39	Y	F7	RW byte	VFDE_ENABLE.
MFR_SPECIFIC_40	Y	F8	RW byte	ULTRASONIC_ENABLE.
MFR_SPECIFIC_41	N*1*	F9	RW byte	GDC_THRESHOLD. To access the internal register to set GDC threshold [A]

Table 11. Supported commands (continued)

Command	Per rail	Code [Hex]	Mode	Comments
MFR_SPECIFIC_42	N*1*	FA	RW byte	DPM12_THRESHOLD. To access the internal register to set the DPM12 threshold [A]
MFR_SPECIFIC_43	N*1*	FB	RW byte	DPM23_THRESHOLD. To access the internal register to set the DPM23 threshold [A]
CAPABILITY	N	19	R byte	It provides a way for a host system to determine key capabilities of a PMBus device, such as maximum bus speed and PMBus alert.
VOUT_MODE	N	20	R byte	The device operates in VID mode.
PMBUS_REVISION	N	98	R byte	Revision of the PMBus which the device is compliant to
MFR_ID	N	99	R block	Returns the manufacturer ID
MFR_MODEL	N	9A	R block	Returns manufacturer model number
MFR_REVISION	N	9B	R block	Returns the device revision number
MFR_SPECIFIC_25	N	E9	R byte	ST_MODEL_ID
MFR_SPECIFIC_EXTENDED_COMMAND_00	Y	00	R byte	VR12_STATUS1
MFR_SPECIFIC_EXTENDED_COMMAND_01	Y	01	R byte	VR12_STATUS2
MFR_SPECIFIC_EXTENDED_COMMAND_02	Y	02	R byte	VR12_TEMPZONE
MFR_SPECIFIC_EXTENDED_COMMAND_03	Y	03	R byte	VR12_IOUT
MFR_SPECIFIC_EXTENDED_COMMAND_05	Y	05	R byte	VR12_VRTEMP
MFR_SPECIFIC_EXTENDED_COMMAND_07	Y	07	R byte	VR12_STATUS2_LASTREAD
MFR_SPECIFIC_EXTENDED_COMMAND_08	Y	08	R byte	VR12_ICCMAX
MFR_SPECIFIC_EXTENDED_COMMAND_09	Y	09	R byte	VR12_TEMPMAX
MFR_SPECIFIC_EXTENDED_COMMAND_10	Y	0A	R byte	VR12_SRFAST
MFR_SPECIFIC_EXTENDED_COMMAND_11	Y	0B	R byte	VR12_SRSLOW
MFR_SPECIFIC_EXTENDED_COMMAND_12	Y	0C	R byte	VR12_VBOOT
MFR_SPECIFIC_EXTENDED_COMMAND_13	Y	0D	R byte	VR12_VOUTMAX
MFR_SPECIFIC_EXTENDED_COMMAND_14	Y	0E	R byte	VR12_VIDSETTING

Table 11. Supported commands (continued)

Command	Per rail	Code [Hex]	Mode	Comments
MFR_SPECIFIC_EXTENDED_COMMAND_15	Y	0F	R byte	VR12_PWRSTATE
MFR_SPECIFIC_EXTENDED_COMMAND_16	Y	10	R byte	VR12_OFFSET
CLEAR_FAULTS	N	03	Send byte	Used to clear any fault bits that have been set
READ_VIN	N	88	R word	Returns the input voltage in volts (VIN pin)
READ_VOUT	Y	8B	R word	Returns the actual reference used for the regulation in VID format.
READ_IOUT	Y	8C	R word	Returns the output current in amps
READ_DUTY_CYCLE	N*1*	94	R word	Returns the duty cycle of the devices' main power converter in percentage
MFR_SPECIFIC_04	Y	D4	R word	READ_VOUT. Returns the actual reference used for the regulation in volts for linear format.
READ_TEMPERATURE_1	Y	8D	R word	READ_TEMPERATURE. [DegC]
STATUS_BYTE	Y	78	R byte	One byte with information on the most critical faults.
STATUS_WORD	Y	79	R word	Two bytes with information on the units' fault condition.
STATUS_VOUT	Y	7A	R byte	Status information on the output voltage warnings and faults.
STATUS_IOUT	Y	7B	R byte	Status information on the output current warnings and faults.
STATUS_TEMPERATURE	Y	7D	R byte	Status information on the temperature warnings and faults.
STATUS_CML	Y	7E	R byte	Status information on the units communication, logic and memory.
STATUS_INPUT	N*1*	7C	R byte	Status information on the input warning and fault
STATUS_MFR_SPECIFIC	Y	80	R byte	Manufacturer specific status

Note: 1 Applies to multi-phase only.
2 Applies to single-phase only.

12.1 Enabling the device through PMBus

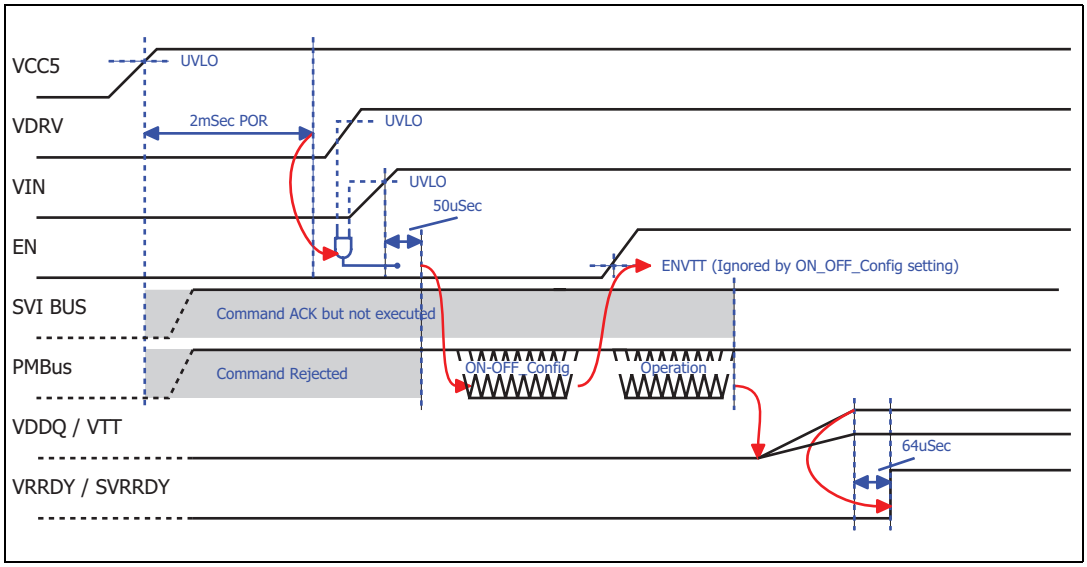
The default condition for the L6759D is to power up through the EN pin ignoring PMBus commands. By properly setting the ON_OFF_CONFIG command, it is also possible to let the device ignore the EN pin acting only as a consequence of the OPERATION command issued.

12.2 Controlling Vout through PMBus

Vout can be set independently from the SetVID commands issued through the SVI interface by using PMBus. Two main modes can be identified:

- Offset above SVI commanded voltage. By enabling the MARGIN mode through the OPERATION command and by commanding the MARGIN_HIGH and MARGIN_LOW registers, it is possible to dynamically control an offset above the output voltage commanded through the SVI bus.
- Fixed Vout regardless of SVI.It is necessary to enter DEBUG_MODE. In this condition, commands from SVI are acknowledged but not executed and VOUT_COMMAND controls the voltage regulated on the output.The L6759D can enter and exit DEBUG_MODE anytime. Upon any transition, Vout remains unchanged and only the next-coming command affects the output voltage positioning (i.e. when exiting DEBUG_MODE, returning to SVI domain, the output voltage remains unchanged until the next SetVID command).

Figure 18. Device initialization: PMBus controlling Vout



12.3 Input voltage monitoring (READ_VIN)

The dedicated PMBus command allows the user to monitor input voltage. By connecting the VIN pin to the input voltage with recommended resistor values, the L6759D returns the value of the input voltage measured as a voltage (linear format, N= -4).

The divider needs to be programmed to have 1.24 V on the pin when VIN=15.9375 V. According to this, R_{UP}=118.5 kΩ and R_{DOWN}=10 kΩ

Errors in defining the divider lead to monitoring errors accordingly.

Filter the VIN pin locally to GND to increase stability of the voltage being measured.

12.4 Duty cycle monitoring (READ_DUTY)

The dedicated PMBus command allows the user to monitor duty cycle for multi-phase with the aim of calculating input current inexpensively (no need for input current sense resistors). By connecting the PHASE pin to the phase1 PHASE pin, the L6759D returns the value of the duty-cycle as a percentage (linear format, N=-2).

The divider needs to be programmed to respect absolute maximum ratings for the pin (7 Vmax). According to this, R_{UP}=5.6 kΩ and R_{DOWN}=470 Ω

12.5 Output voltage monitoring (READ_VOUT)

The dedicated PMBus command allows the user to monitor the output voltage for both sections. The L6759D returns the value of the programmed VID in VID LSBs (i.e. number of LSBs. C8h = 200 dec x 5 mV = 1.000 V).

12.6 Output current monitoring (READ_IOUT)

The dedicated PMBus command allows the user to monitor the output current for the multi-phase section. The L6759D returns the value of the delivered current by reading IMON voltage (same as VR12 Register 15h) in amperes (linear format, N=0).

12.7 Temperature monitoring (READ_TEMPERATURE)

The dedicated PMBus command allows the user to monitor the temperature of the power section for multi-phase. The L6759D returns the value of the temperature sensed by NTC connected on the TM pin (the same as VR12 temperature zone) in celsius degrees (linear format, N=0).

12.8 Overvoltage threshold setting

The dedicated MFR_SPECIFIC command allows the programming of a specific threshold for multi-phase and single-phase sections.

The threshold can be programmed according to *Table 12*. Different thresholds can be configured for multi-phase and single-phase sections.

Table 12. OV threshold setting

Data byte [Hex]	OC threshold [mV] (above programmed VID)
00h	+175 mV (default)
01h	+225 mV
02h	+275 mV
03h	+325 mV

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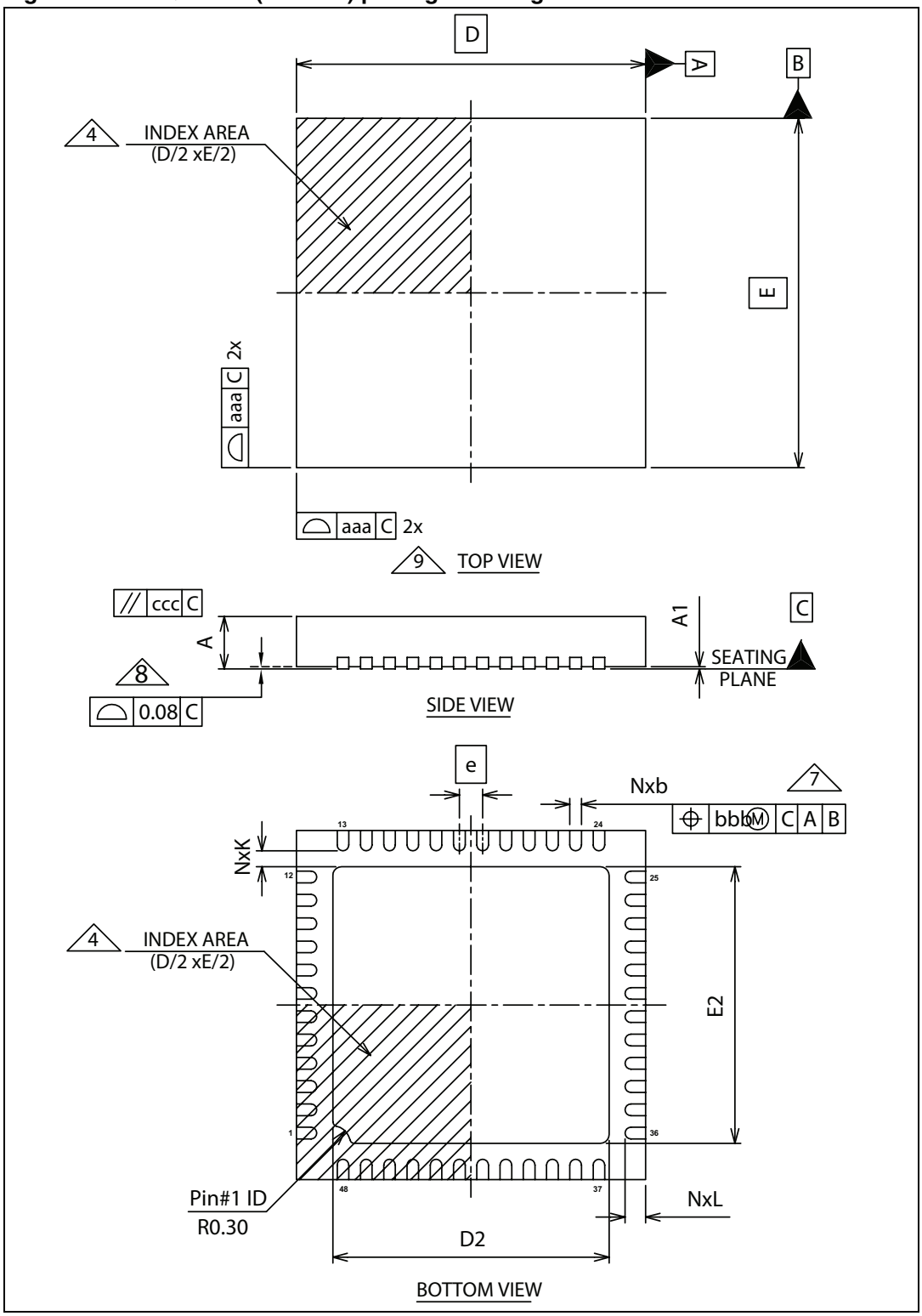
13 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 13. VFQFPN48 (6x6 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
D		6.00	
D2			4.40
E		6.00	
E2			4.40
b	0.15	0.20	0.25
e		0.40	
k	0.20		
L	0.25	0.35	0.45
aaa		0.10	
bbb		0.07	
ccc		0.10	

Figure 19. VFQFPN48 (6x6 mm) package drawing



14 Revision history

Table 14. Document revision history

Date	Revision	Changes
31-May-2012	1	Initial release.

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